

FEATURES

- 16 channel dual simultaneously sampled inputs
- Independently selectable channel input ranges
 - True bipolar: $\pm 10\text{ V}$, $\pm 5\text{ V}$, $\pm 2.5\text{ V}$
- Single 5 V analog supply and 2.3 V to 5.25 V V_{DRIVE}
- Fully integrated data acquisition solution
 - Analog input clamp protection
 - Input buffer with 1 M Ω analog input impedance
 - First-order antialiasing analog filter
 - On-chip accurate reference and reference buffer
 - Dual 16-bit SAR ADC
 - Throughput rate: $2 \times 1\text{ MSPS}$
 - Oversampling capability with digital filter
 - Flexible sequencer with burst mode
- Flexible parallel/serial interface
 - SPI/QSPI™/MICROWIRE/DSP-compatible
 - Optional CRC error checking
- Hardware/software configuration
- Performance
 - 92 dB SNR at 500 kSPS (2 \times oversampling)
 - 90 dB SNR at 1 MSPS
 - 103 dB THD
 - $\pm 2\text{ LSB INL}$, $\pm 0.99\text{ LSB DNL}$
 - 8 kV ESD rating on analog input channels
- On-chip self-detect function
- 80-lead LQFP package

APPLICATIONS

- Power line monitoring
- Protective relays
- Multiphase motor control
- Instrumentation and control systems
- Data acquisition systems (DAS)

GENERAL DESCRIPTION

The AD7616 is a 16-bit, data acquisition system (DAS) that supports dual simultaneous sampling of 16 channels. The AD7616 operates from a single 5 V supply and can accommodate $\pm 10\text{ V}$, $\pm 5\text{ V}$, and $\pm 2.5\text{ V}$ true bipolar input signals while sampling at throughput rates up to 1 MSPS per channel pair with 90 dB SNR. Higher SNR performance can be achieved with the on-chip oversampling mode; 92 dB for an oversampling ratio of 2.

The input clamp protection circuitry can tolerate voltages up to $\pm 20\text{ V}$. The AD7616 has 1 M Ω analog input impedance regardless of sampling frequency. The single supply operation, on-chip filtering, and high input impedance eliminate the need for driver op amps and external bipolar supplies.

Each device contains analog input clamp protection, a dual, 16-bit charge redistribution successive approximation analog-to-digital converter (ADC), a flexible digital filter, a 2.5 V reference and reference buffer, and high speed serial and parallel interfaces.

FUNCTIONAL BLOCK DIAGRAM

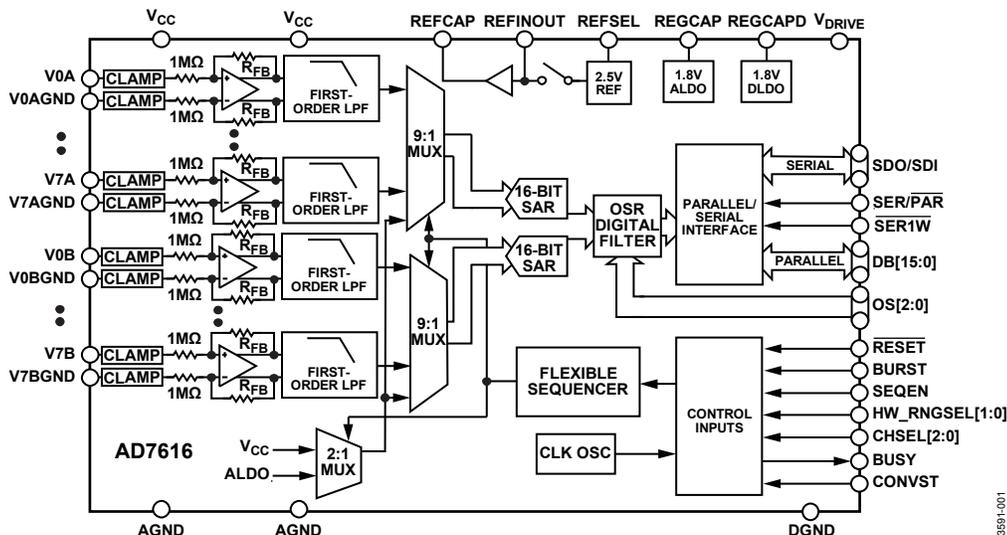


Figure 1.

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SPECIFICATIONS

$V_{REF} = 2.5$ V external/internal, $V_{CC} = 4.75$ V to 5.25 V, $V_{DRIVE} = 2.3$ V to 5.25 V, $f_{SAMPLE} = 1$ MSPS, $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, unless otherwise noted. Note that throughout this data sheet, multifunction pins, such as SCLK/RD, are referred to either by the entire pin name or by a single function of the pin, for example, SCLK, when only that function is relevant.

Table 1.¹

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit	
DYNAMIC PERFORMANCE						
Signal-to-Noise Ratio (SNR) ^{2, 3}	$f_{IN} = 1$ kHz sine wave unless otherwise noted					
	No oversampling, ± 10 V range	87.5	90		dB	
	OSR = 2, ± 10 V range		92		dB	
Signal-to-Noise-and-Distortion (SINAD)	OSR = 4, ± 10 V range		93		dB	
	No oversampling, ± 5 V range	86.5	89		dB	
	No oversampling, ± 2.5 V range	83.5	87		dB	
	No oversampling, ± 10 V range	87	90		dB	
	No oversampling, ± 5 V range	86.5	89		dB	
Dynamic Range	No oversampling, ± 2.5 V range	83	87		dB	
	No oversampling, ± 10 V range		92		dB	
	No oversampling, ± 5 V range		90.5		dB	
	No oversampling, ± 2.5 V range		88		dB	
Total Harmonic Distortion (THD)			-103	-95	dB	
Peak Harmonic or Spurious Noise (SFDR)			-103		dB	
Intermodulation Distortion (IMD)	$f_a = 1$ kHz, $f_b = 1.1$ kHz					
Second-Order Terms			-104		dB	
Third-Order Terms			-102		dB	
Channel to Channel Isolation	f_{IN} on unselected channels up to 5 kHz		-106		dB	
ANALOG INPUT FILTER						
Full Power Bandwidth	-3 dB		35		kHz	
$t_{GROUP\ DELAY}$	-0.1 dB	5.3	5.5		kHz	
	± 10 V range		4.6	5	μs	
	± 5 V range		5.4		μs	
$t_{GROUP\ DELAY\ Drift}$	± 2.5 V range		5.6		μs	
	± 10 V range		TBD	TBD	ns/ $^{\circ}\text{C}$	
	± 5 V range		TBD		ns/ $^{\circ}\text{C}$	
$t_{GROUP\ DELAY\ MATCHING}$ (Dual Simultaneous Pair)	± 2.5 V range		TBD		ns/ $^{\circ}\text{C}$	
	± 10 V range		TBD	100	ns	
	± 5 V range		TBD		ns	
DC ACCURACY	± 2.5 V range		TBD		ns	
	Resolution	No missing codes	16		Bits	
	Differential Nonlinearity (DNL)			± 0.65	± 0.99	LSB ⁴
	Integral Nonlinearity (INL)			± 2	± 4	LSB
	Total Unadjusted Error (TUE)	± 10 V range		± 6		LSB
		± 5 V range		± 12		LSB
		± 2.5 V range		± 24		LSB
	Positive Full-Scale Error	External reference		± 2	± 32	LSB
		Internal reference		± 3		LSB
	Positive Full-Scale Error Drift	External reference		± 2	± 10	ppm/ $^{\circ}\text{C}$
Internal reference			± 8		ppm/ $^{\circ}\text{C}$	
Positive Full-Scale Error Matching	± 10 V range		3	32	LSB	
	± 5 V range		16	40	LSB	
	± 2.5 V range		30		LSB	

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Bipolar Zero Code Error	±10 V range		±0.7	±6	LSB
	± 5 V range		±3	±12	LSB
	±2.5 V range		±6	±24	LSB
Bipolar Zero Code Error Drift	±10 V range		8.6		μV/°C
	± 5 V range		5		μV/°C
	±2.5 V range		2.5		μV/°C
Bipolar Zero Code Error Matching	±10 V range		2	8	LSB
	±5 V range		6	22	LSB
	±2.5 V range		12		LSB
Negative Full-Scale Error	External reference		±1.3	±32	LSB
	Internal reference		±2.8		LSB
Negative Full-Scale Error Drift	External reference		±1	±10	ppm/°C
	Internal reference		±4		ppm/°C
Negative Full-Scale Error Matching	±10 V range		2.3	32	LSB
	±5 V range		16	40	LSB
	±2.5 V range		30		LSB
ANALOG INPUT					
Input Voltage Ranges	Software/hardware selectable			±10	V
	Software/hardware selectable			±5	V
	Software/hardware selectable			±2.5	V
Analog Input Current			$I_{AIN} = (0.866 \times V_{IN}) - 1.945$		μA
Input Capacitance ⁵			10		pF
Input Impedance	See the Analog Input section	0.85	1	1.15	MΩ
Input Impedance Drift				50	ppm/°C
REFERENCE INPUT/OUTPUT					
Reference Input Voltage Range	See the ADC Transfer Function section	2.475	2.5	2.525	V
DC Leakage Current				±1	μA
Input Capacitance ⁵	REF SELECT = 1		7.5		pF
Reference Output Voltage	REFIN to REFOUT		2.495 to 2.505		V
Reference Temperature Coefficient			±10	±15	ppm/°C
LOGIC INPUTS					
Input Voltage High (V _{INH})	V _{DRIVE} = 2.7 V to 5.25 V	2			V
	V _{DRIVE} = 2.3 V to 2.7 V	1.7			V
Input Voltage Low (V _{INL})	V _{DRIVE} = 2.7 V to 5.25 V			0.8	V
	V _{DRIVE} = 2.3 V to 2.7 V			0.7	V
Input Current (I _{IN})				±1	μA
Input Capacitance (C _{IN}) ⁵			5		pF
LOGIC OUTPUTS					
Output Voltage High (V _{OH})	I _{SOURCE} = 100 μA	V _{DRIVE} - 0.2			V
			Low (V _{OL})		0.4
Floating State Leakage Current	I _{SINK} = 100 μA		±0.5	±1	μA
Floating State Output Capacitance ⁵			5		pF
Output Coding	Twos complement				
CONVERSION RATE					
Conversion Time	Per channel pair		0.5		μs
Acquisition Time	Per channel pair		0.5		μs
Throughput Rate	Per channel pair			1	MSPS

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER REQUIREMENTS					
V _{CC}		4.75		5.25	V
V _{DRIVE}		2.3		5.25	V
I _{VCC}					
Normal Mode (Static)			37	55	mA
Normal Mode (Operational)	f _{SAMPLE} = 1 MSPS		44	65	mA
Shutdown Mode			100	150	μA
I _{DRIVE}	Digital inputs = 0 V or V _{DRIVE}				
Normal Mode (Static)			0.3	0.4	mA
Normal Mode (Operational)	f _{SAMPLE} = 1 MSPS		7	8	mA
Shutdown Mode			50	150	μA
Power Dissipation					
Normal Mode (Static)			187	295	mW
Normal Mode (Operational)	f _{SAMPLE} = 1 MSPS		268	385	mW
Shutdown Mode			0.75		mW

¹ All specifications are TBD until full product release.

² See the Terminology section.

³ The user can achieve 93 dB SNR by enabling OS. The values are valid for manual mode. In burst mode, values degrade by ~1 dB.

⁴ LSB means least significant bit. With a ±2.5 V input range, 1 LSB = 76.293 μV. With a ±5 V input range, 1 LSB = 152.58 μV. With a ±10 V input range, 1 LSB = 305.175 μV.

⁵ Sample tested during initial release to ensure compliance.

TIMING SPECIFICATIONS

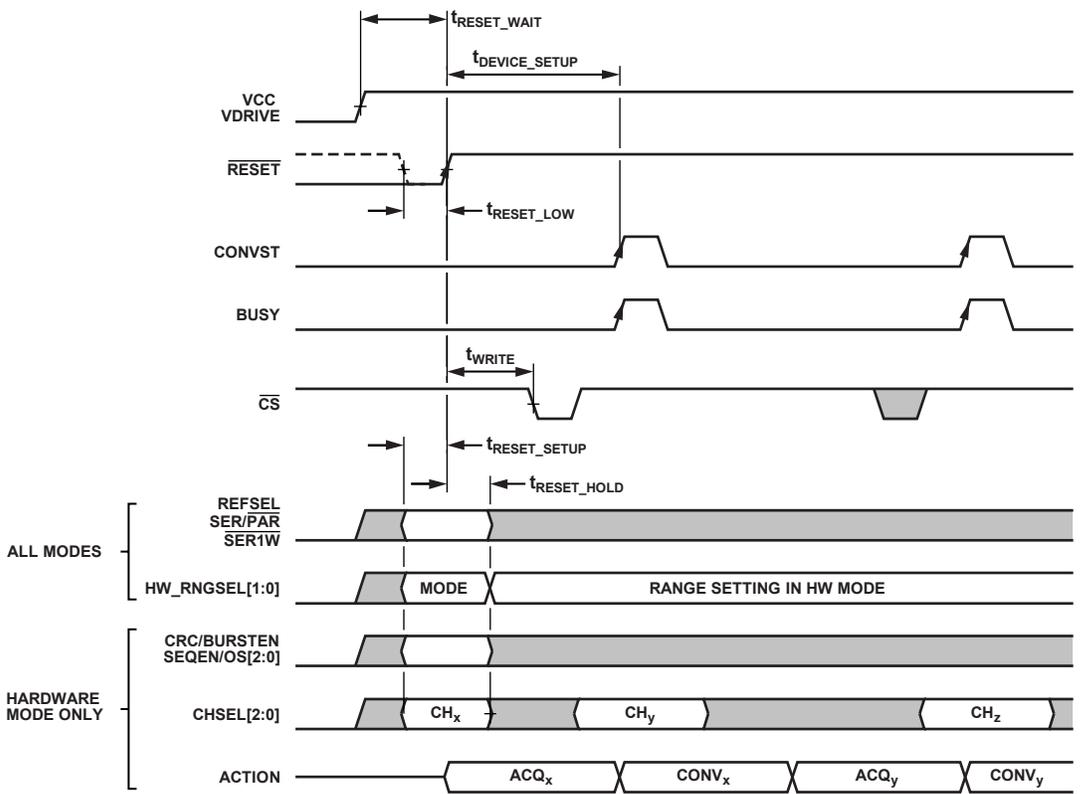
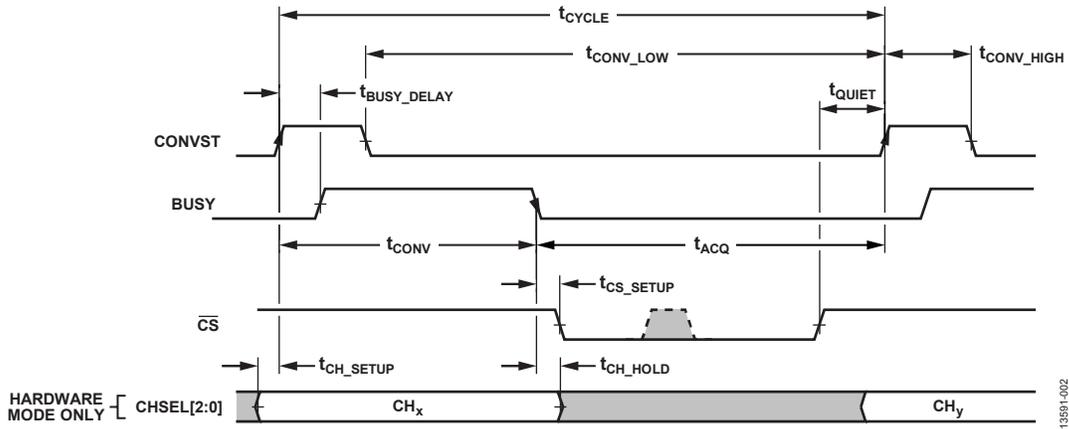
V_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 2.3 V to 5.25 V, V_{REF} = 2.5 V external reference/internal reference, T_A = -40 to +125°C, unless otherwise noted.

Table 2. Universal Timing Specifications^{1, 2}

Parameter	Min	Typ	Max	Unit	Description
t _{CYCLE}	1			μs	Minimum time between consecutive CONVST rising edges (excluding burst and oversampling modes)
t _{CONV_LOW}	20			ns	CONVST low pulse width
t _{CONV_HIGH}	20			ns	CONVST high pulse width
t _{BUSY_DELAY}			40	ns	CONVST high to BUSY high
t _{CS_SETUP}			20	ns	BUSY falling edge to \overline{CS} falling edge setup time
t _{CH_SETUP}			200	ns	Channel select setup time in hardware mode for CHSELx
t _{CH_HOLD}			20	ns	Channel select hold time in hardware mode for CHSELx
t _{CONV}		450	500	ns	Conversion time for the selected channel pair
t _{ACQ}	500			ns	Acquisition time for the selected channel pair
t _{QUIET}	80			ns	\overline{CS} rising edge to next CONVST rising edge
t _{RESET_LOW}					
Partial Reset	40		500	ns	Partial \overline{RESET} low pulse width
Full Reset	1200			ns	Full \overline{RESET} low pulse width
t _{DEVICE_SETUP}					
Partial Reset	50			ns	Minimum delay between partial \overline{RESET} high to CONVST rising edge
Full Reset	15			ms	Minimum delay between full \overline{RESET} high to CONVST rising edge
t _{WRITE}					
Partial Reset	50			ns	Minimum delay between partial \overline{RESET} high to \overline{CS} for write operation
Full Reset	240			μs	Minimum delay between full \overline{RESET} high to \overline{CS} for write operation
t _{RESET_WAIT}	1			ms	Minimum time between stable V _{CC} /V _{DRIVE} to release of \overline{RESET} (see Figure 14)
t _{RESET_SETUP}	0.05			ms	Minimum time before deassertion of \overline{RESET} that queried hardware inputs must be stable for (see Figure 14)
t _{RESET_HOLD}	0.24			ms	Minimum time after deassertion of \overline{RESET} that queried hardware inputs must be stable for (see Figure 14)

¹ All timing specifications are TBD until product release.

² Sample tested during initial release to ensure compliance.



PARALLEL MODE TIMING SPECIFICATIONS

Table 3. Parallel Mode¹

Parameter	Min	Typ	Max	Unit	Description
t_{RD_SETUP}	10			ns	\overline{CS} falling edge to \overline{RD} falling edge setup time
t_{RD_HOLD}	10			ns	\overline{RD} rising edge to \overline{CS} rising edge hold time
t_{RD_HIGH}	30			ns	\overline{RD} low pulse width
t_{RD_LOW}	40			ns	\overline{RD} high pulse width
t_{DOUT_SETUP}			40	ns	Data access time after falling edge of \overline{RD} , V_{DRIVE} above 4.75 V
t_{DOUT_HOLD}			10	ns	Data hold time after rising edge of \overline{RD}
t_{DOUT_3STATE}			10	ns	\overline{CS} rising edge to DBx high impedance
t_{WR_SETUP}	10			ns	\overline{CS} to \overline{WR} setup time
t_{WR_HIGH}	30			ns	\overline{WR} high pulse width
t_{WR_LOW}	40			ns	\overline{WR} low pulse width
t_{DIN_SETUP}	40			ns	Configuration data to \overline{WR} setup time
t_{DIN_HOLD}	10			ns	Configuration data to \overline{WR} hold time
t_{CONF_SETTLE}	30			ns	Configuration data settle time, \overline{WR} rising edge to CONVST rising edge

¹ All timing specifications are TBD until product release.

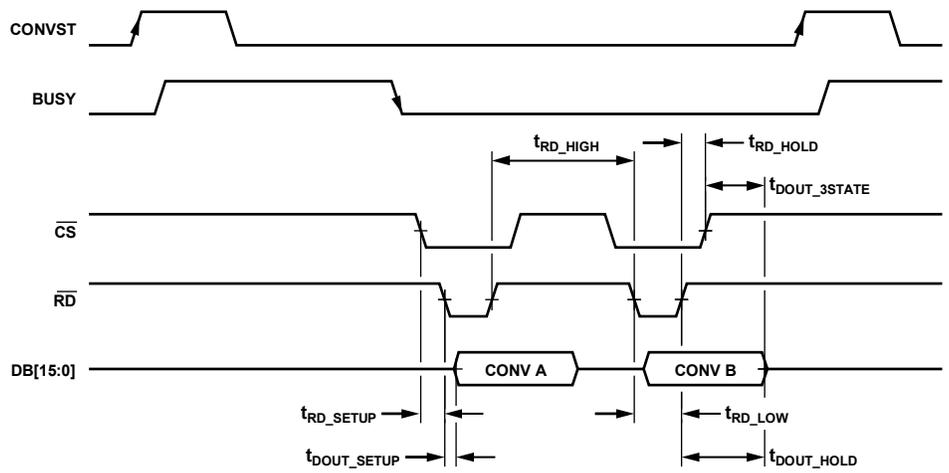


Figure 4. Parallel Read Timing

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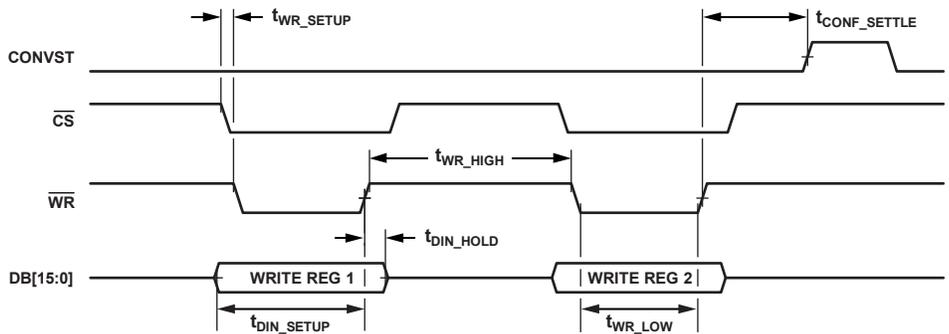


Figure 5. Parallel Write Timing

13591-034

SERIAL MODE TIMING SPECIFICATIONS

Table 4. Serial Mode¹

Parameter	Min	Typ	Max	Unit	Description
t _{SCLK_SETUP}	10			ns	\overline{CS} to SCLK falling edge setup time
t _{SCLK_HOLD}	10			ns	SCLK to \overline{CS} rising edge hold time
t _{SCLK}	40		50	MHz	SCLK frequency ²
t _{SCLK_LOW}	10			ns	SCLK low pulse width
t _{SCLK_HIGH}	10			ns	SCLK high pulse width
t _{MSB_SETUP}			10	ns	MSB access time after \overline{CS} falling edge
t _{DOUT_SETUP}			10	ns	Data out access time after SCLK rising edge, V _{DRIVE} above 4.75 V
			10	ns	Data out access time after SCLK rising edge, V _{DRIVE} above 3.3 V
			12.5	ns	Data out access time after SCLK rising edge, V _{DRIVE} above 2.7 V
			12.5	ns	Data out access time after SCLK rising edge, V _{DRIVE} above 2.3 V
t _{DOUT_HOLD}			4	ns	Data out hold time after SCLK rising edge
t _{DIN_SETUP}			10	ns	Data in setup time before SCLK falling edge
t _{DIN_HOLD}	8			ns	Data in hold time after SCLK falling edge
t _{DOUT_3STATE}	10			ns	\overline{CS} rising edge to SDO high impedance

¹ All timing specifications are TBD until product release.
² Dependent on V_{DRIVE} and load capacitance (see Table 14).

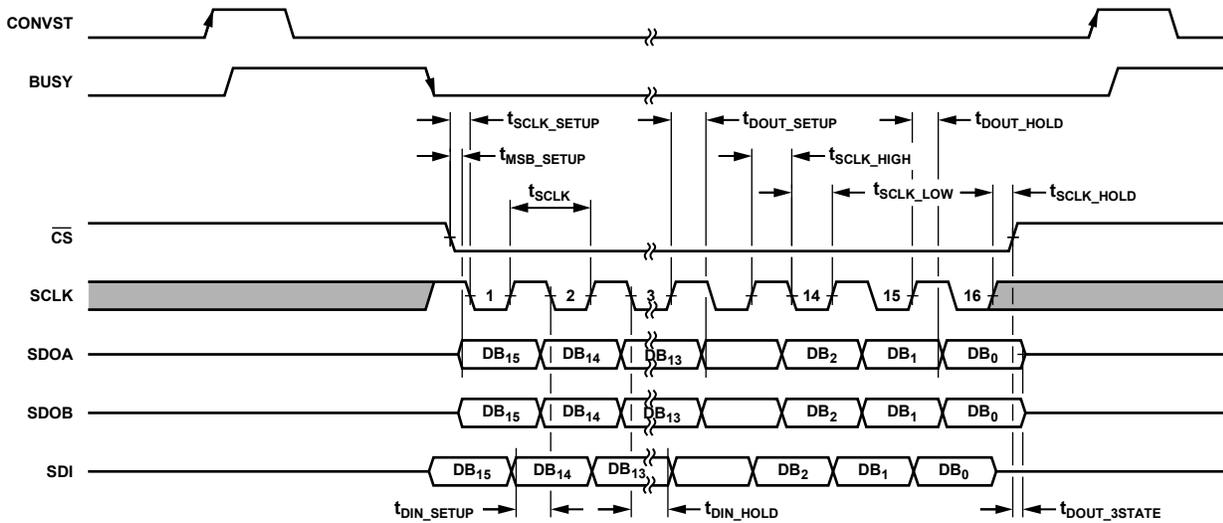


Figure 6. Serial Timing

13551-004

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V _{CC} to AGND	-0.3 V to +7 V
V _{DRIVE} to AGND	-0.3 V to V _{CC} + 0.3 V
Analog Input Voltage to AGND ¹	±21 V
Digital Input Voltage to AGND	-0.3 V to V _{DRIVE} + 0.3 V
Digital Output Voltage to AGND	-0.3 V to V _{DRIVE} + 0.3 V
REFIN to AGND	-0.3 V to V _{CC} + 0.3 V
Input Current to Any Pin Except Supplies ¹	±10 mA
Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
Soldering Reflow	
Pb/SN Temperature (10 sec to 30 sec)	240 (+0)°C
Pb-Free Temperature	260 (+0)°C
ESD	
All Pins Except Analog Inputs	2 kV
Analog Input Pins Only	8 kV

¹ Transient currents of up to 100 mA do not cause silicon-controlled rectifier (SCR) latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Table 6. Thermal Resistance

Package Type	θ _{JA}	θ _{JB}	θ _{JC}	ψ _{JT}	ψ _{JB}	Unit
80-Lead LQFP ¹	41	23	7.5	0.38	22.5	°C/W

¹ Thermal impedance simulated values are based on JEDEC 2S2P thermal test board. See JEDEC JESD51

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

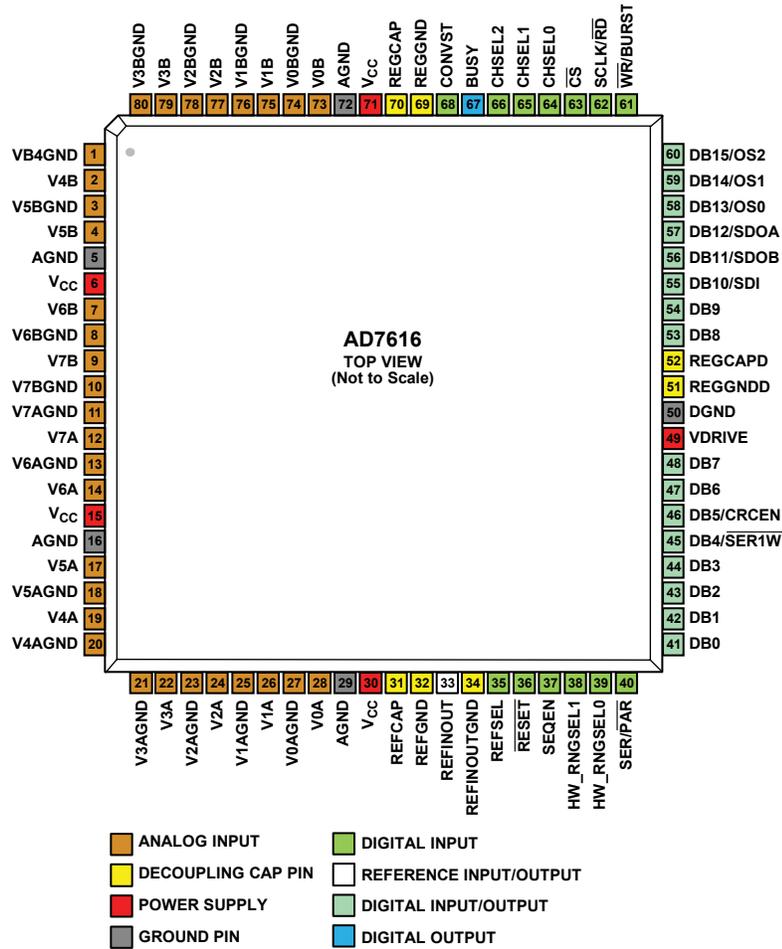


Figure 7. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Type ¹	Mnemonic	Description
1	AI GND	V4BGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V4B.
2	AI	V4B	Analog Input V4B.
3	AI GND	V5BGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V5B.
4	AI	V5B	Analog Input V5B.
5, 16, 29, 72	P	AGND	Analog Supply Ground Pins.
6, 15, 30, 71	P	V _{CC}	Analog Supply Voltage, 4.7 V to 5.25 V. This supply voltage is applied to the internal front-end amplifiers and to the ADC core. Decouple these pins to AGND.
7	AI	V6B	Analog Input V6B.
8	AI GND	V6BGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin t V6B.
9	AI	V7B	Analog Input V7B.
10	AI GND	V7BGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V7B.
11	AI GND	V7AGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V7A.
12	AI	V7A	Analog Input V7A.
13	AI GND	V6AGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V6A.
14	AI	V6A	Analog Input V6A.
17	AI	V5A	Analog Input V5A.
18	AI GND	V5AGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V5A.
19	AI	V4A	Analog Input V4A.
20	AI GND	V4AGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V4A.

Pin No.	Type ¹	Mnemonic	Description
21	AI GND	V3AGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V3A.
22	AI	V3A	Analog Input V3A.
23	AI GND	V2AGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V2A.
24	AI	V2A	Analog Input V2A.
25	AI GND	V1AGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V1A.
26	AI	VA1	Analog Input V1A.
27	AI GND	VOAGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V0A.
28	AI	V0A	Analog Input V0A
31	REF	REFCAP	Reference Buffer Output Force/Sense Pins. This pin must be decoupled to AGND using a low ESR, 10 μ F ceramic capacitor. The voltage on this pin is typically 4.096 V.
32	REF	REFGND	Reference Ground pin. This pin should be connected to AGND.
33	REF	REFINOUT	Reference Input/Reference Output. The on-chip reference of 2.5 V is available on this pin for external use if the REFSEL pin is set to logic high. Alternatively, the internal reference can be disabled by setting the REFSEL pin to logic low, and an external reference of 2.5 V can be applied to this input. Decoupling is required on this pin for both the internal and external reference options. Connect a 100 nF capacitor from this pin to AGND close to the REFINOUTGND pin. If using an external reference, connect a 10 k Ω series resistor to this pin to band limit the reference signal.
34	REF	REFINOUTGND	Reference Input, Reference Output Ground Pin.
35	DI	REFSEL	Internal/External Reference Selection Input. Logic input. If this pin is set to logic high, the internal reference is selected and enabled. If this pin is set to logic low, the internal reference is disabled and an external reference voltage must be applied to the REFINOUT pin. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure.
36	DI	$\overline{\text{RESET}}$	Reset Input. <u>Full and partial reset options</u> are available. The type of reset is determined by the length of the RESET pulse. Keeping RESET low places the device into shutdown mode. See the Reset Functionality section for further details.
37	DI	SEQEN	Channel Sequencer Enable Input (Hardware Mode Only). When SEQEN is tied low, the sequencer is disabled. When SEQEN is high, the sequencer is enabled (with restricted functionality in hardware mode). See the Sequencer section for further details. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure. In software mode, this pin must be connected to DGND.
38, 39	DI	HW_RNGSEL0, HW_RNGSEL1	Hardware/Software Mode Selection, Hardware Mode Range Select Inputs. Hardware/software mode selection is latched at full reset. Range selection in hardware mode is not latched. HW_RNGSELx = 00: software mode; the AD7616 is configured via the software registers. HW_RNGSELx = 01: hardware mode; analog input range is ± 2.5 V. HW_RNGSELx = 10: hardware mode; analog input range is ± 5 V. HW_RNGSELx = 11: hardware mode; analog input range is ± 10 V.
40	DI	$\overline{\text{SER/PAR}}$	Serial/Parallel Interface Selection Input. Logic input. If this pin is tied to a logic low, the parallel interface is selected. If this pin is tied to logic high, the serial interface is selected. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure.
41, 42, 43, 44	DO/DI	DB0, DB1, DB2, DB3	Parallel Output/Input Data Bits. In parallel mode, these pins are output/input parallel data bits, DB7 to DB0. Refer to the Parallel Interface section for further details. In serial mode, these pins must be tied to DGND.
45	DO/DI	DB4/ $\overline{\text{SER1W}}$	Digital Output/Input. In parallel mode, this pin acts as a three-state parallel digital output/input pin. Refer to the Parallel Interface section for further details. In serial mode, this pin determines if the serial output operates over SDOA and SDOB or just SDOA. When $\overline{\text{SER1W}}$ is low, the serial output operates over SDOA only. When SER1W is high, the serial output operates over both SDOA and SDOB. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure.
46	DO/DI	DB5/CRCEN	Parallel Output/Input Data Bit/CRC Enable Input. In parallel mode, this pin acts as a three-state parallel digital input/output. While in serial mode, this pin acts as CRCEN input. The CRCEN signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure. Refer to the Digital Interface section for further details. In serial mode, when CRCEN is low, there is no CRC word following the conversion results; when CRCEN is high, an extra CRC word follows the last conversion word configured by CHSELx. See the CRC section for further details. In software mode, this pin must be connected to DGND.

Pin No.	Type ¹	Mnemonic	Description
47, 48	DO/DI	DB6, DB7	Parallel Output/Input Data Bits. When $\overline{\text{SER/PAR}} = 0$, these pins act as three-state parallel digital input/outputs. Refer to the Parallel Interface section for further details. In serial mode, when $\overline{\text{SER/PAR}} = 1$ these pins must be tied to DGND.
49	P	VDRIVE	Logic Power Supply Input. The voltage (2.3 V to 5.25 V) supplied at this pin determines the operating voltage of the interface. This pin is nominally at the same supply as the supply of the host interface.
50	P	DGND	Digital Ground. This pin is the ground reference point for all digital circuitry on the AD7616. DGND must connect to the DGND plane of a system.
51	P	REGGND	Ground for the Digital LDO Connected to REGCAPD (Pin 52).
52	P	REGCAPD	Decoupling Capacitor Pin for Voltage Output from Internal Digital Regulator. Decouple this output pin separately to REGGND using a 10 μF capacitor. The voltage at this pin is 1.8V typical.
54,53	DO/DI	DB9, DB8	Parallel Output/Input Data Bits. When $\overline{\text{SER/PAR}} = 0$, this pin acts as a three-state parallel digital input/output. Refer to the Parallel Interface section for further details. In serial mode, when $\overline{\text{SER/PAR}} = 1$ these pins must be tied to DGND,
55	DO/DI	DB10/SDI	Parallel Output/Input Data Bit DB10/Serial Data Input. When $\overline{\text{SER/PAR}} = 0$, this pin acts as a three-state parallel digital input/output. Refer to the Parallel Interface section for further details. In serial mode, when $\overline{\text{SER/PAR}} = 1$ this pin acts as the data input of the SPI interface.
56	DO/DI	DB11/SDOB	Parallel Output/Input Data Bit/Serial Data Output B. When $\overline{\text{SER/PAR}} = 0$, this pin acts as a three-state parallel digital input/output. Refer to the Parallel Interface section for further details. In serial mode, when $\overline{\text{SER/PAR}} = 1$ this pin functions as SDOB and outputs serial conversion data.
57	DO/DI	DB12/SDOA	Parallel Output/Input Data Bit/Serial Data Output A. When $\overline{\text{SER/PAR}} = 0$, this pin acts as a three-state parallel digital input/output. Refer to the Parallel Interface section for further details. In serial mode, when $\overline{\text{SER/PAR}} = 1$ this pin functions as SDOA and outputs serial conversion data.
58, 59, 60	DO/DI	DB13/OS0, DB14/OS1, DB15/OS2	Parallel Output/Input Data Bits/Oversampling Ratio Selection. When $\overline{\text{SER/PAR}} = 0$, these pins act as three-state parallel digital input/outputs. Refer to the Parallel Interface section for further details. In serial hardware mode, these pins control the oversampling settings. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure. See the Digital Filter section for further details. In software serial mode, these pins must be connected to DGND.
61	DI	$\overline{\text{WR}}$ /BURST	Write/Burst Mode Enable. In software parallel mode, this pin acts as $\overline{\text{WR}}$ for a parallel interface. In hardware parallel or serial mode, this pin enables BURST mode. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure. Refer to the Burst Sequencer section for further information. In software serial mode this pin should be connected to DGND.
62	DI	SCLK/ $\overline{\text{RD}}$	Serial Clock Input/Parallel Data Read Control Input. In serial mode, this pin acts as the serial clock input for data transfers. The $\overline{\text{CS}}$ falling edge takes the SDOA and SDOB data output lines out of three-state and clocks out the MSB of the conversion result. The rising edge of SCLK clocks all subsequent data bits onto the SDOA and SDOB serial data outputs. When both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are logic low in parallel mode, the output bus is enabled.
63	DI	$\overline{\text{CS}}$	Chip Select. This active low logic input frames the data transfer. In parallel mode, when both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are logic low, the DBx output bus is enabled and the conversion result is output on the parallel data bus lines. In serial mode, $\overline{\text{CS}}$ frames the serial read transfer and clocks out the MSB of the serial output data.
64, 65, 66	DI	CHSEL0, CHSEL1, CHSEL2	Channel Selection Inputs. In hardware mode, these inputs select the input channels for the next conversion in Channel Group A and Channel Group B. (For example, CHSELx = 0x000 selects VOA and VOB for the next conversion; CHSELx = 0x001 selects V1A and V1B for the next conversion). In software mode, these pins must be connected to DGND.

Pin No.	Type ¹	Mnemonic	Description
67	DO	BUSY	Busy Output. This pin transitions to a logic high after a CONVST rising edge and indicates that the conversion process has started. The BUSY output remains high until the conversion process for the current selected channels is complete. The falling edge of BUSY signals that the conversion data is being latched into the output data registers and is available to read. Data must be read after BUSY returns to low. Rising edges on CONVST have no effect while the BUSY signal is high.
68	DI	CONVST	Conversion Start Input for Channel Group A and Channel Group B. This logic input initiates conversions on the analog input channels. A conversion is initiated when CONVST transitions from low to high for the selected analog input pair. When burst mode and oversampling mode are disabled, every CONVST transition from low to high converts one channel pair. In sequencer mode, when burst mode or oversampling are enabled, a single CONVST transition from low to high is necessary to perform the required number of conversions.
69	P	REGGND	Internal Analog Regulator Ground. This pin must connect to the AGND plane of a system.
70	P	REGCAP	Decoupling Capacitor Pin for Voltage Output from Internal Analog Regulator. Decouple this output pin separately to REGGND using a 10 μ F capacitor. The voltage at this pin is 1.8 V typical.
73	AI	V0B	Analog Input V0B.
74	AI GND	V0BGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V0B.
75	AI	V1B	Analog Input V1B.
76	AI GND	V1BGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V1B.
77	AI	V2B	Analog Input V2B.
78	AI GND	V2BGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V2B.
79	AI	V3B	Analog Input V3B.
80	AI GND	V3BGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V3B.

¹ AI is analog input, GND is ground, P is power supply, REF is reference input/output, DI is digital input, and DO is digital output.

TERMINOLOGY

Integral Nonlinearity

The maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, at $\frac{1}{2}$ LSB below the first code transition; and full scale, at $\frac{1}{2}$ LSB above the last code transition.

Differential Nonlinearity

The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Bipolar Zero Code Error

The deviation of the midscale transition (all 1s to all 0s) from the ideal, which is $0\text{ V} - \frac{1}{2}$ LSB.

Bipolar Zero Code Error Match

The absolute difference in bipolar zero code error between any two input channels.

Positive Full-Scale Error

The deviation of the actual last code transition from the ideal last code transition ($10\text{ V} - 1\frac{1}{2}$ LSB (9.99954), $5\text{ V} - 1\frac{1}{2}$ LSB (4.99977) and $2.5\text{ V} - 1\frac{1}{2}$ LSB (2.49989)) after bipolar zero code error is adjusted out. The positive full-scale error includes the contribution from the internal reference buffer.

Positive Full-Scale Error Match

The absolute difference in positive full-scale error between any two input channels.

Negative Full-Scale Error

The deviation of the first code transition from the ideal first code transition ($-10\text{ V} + \frac{1}{2}$ LSB (-9.99985), $-5\text{ V} + \frac{1}{2}$ LSB (-4.99992) and $-2.5\text{ V} + \frac{1}{2}$ LSB (-2.49996)) after the bipolar zero code error is adjusted out. The negative full-scale error includes the contribution from the internal reference buffer.

Negative Full-Scale Error Match

The absolute difference in negative full-scale error between any two input channels.

Signal-to-Noise-and-Distortion Ratio (SINAD)

SINAD is the measured ratio of signal to noise and distortion at the output of the ADC. The signal is the rms value of the sine wave, and noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_s/2$), including harmonics, but excluding dc.

Signal-to-Noise Ratio (SNR)

SNR is the measured ratio of signal to noise at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_s/2$), excluding dc.

The ratio is dependent on the number of quantization levels in the digitization process: the greater the number of levels, the smaller the quantization noise. The theoretical signal-to-noise ratio for an ideal N-bit converter with a sine wave input is given by

$$\text{Signal-to-Noise Ratio} = (6.02N + 1.76) \text{ dB}$$

Therefore, for a 16-bit converter, the SNR is 98 dB.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels (dB).

Peak Harmonic or Spurious Noise

The ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_s/2$, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is determined by a noise peak.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, f_a and f_b , any active device with nonlinearities creates distortion products at sum and difference frequencies of $m f_a \pm n f_b$, where $m, n = 0, 1, 2, 3$. Intermodulation distortion terms are those for which neither m nor n is equal to 0. For example, the second-order terms include $(f_a + f_b)$ and $(f_a - f_b)$, and the third-order terms include $(2f_a + f_b)$, $(2f_a - f_b)$, $(f_a + 2f_b)$, and $(f_a - 2f_b)$.

The calculation of the intermodulation distortion is per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels (dB).

Power Supply Rejection Ratio (PSRR)

Variations in power supply affect the full-scale transition but not the converter's linearity. PSR is the maximum change in full-scale transition point due to a change in power supply voltage from the nominal value. The PSR ratio (PSRR) is defined as the ratio of the power in the ADC output at full-scale frequency, f , to the power of a 100 mV p-p sine wave applied to the ADC's V_{CC} of Frequency f_s .

$$\text{PSRR (dB)} = 10\log(P_f/P_{f_s})$$

where:

P_f is equal to the power at frequency f in the ADC output.

P_{f_s} is equal to the power at frequency f_s coupled onto the V_{CC} supply.

Channel-to-Channel Isolation

Channel-to-channel isolation is a measure of the level of crosstalk between all input channels. It is measured by applying a full-scale sine wave signal, up to 160 kHz, to all unselected input channels and then determining the degree to which the signal attenuates in the selected channel with a 1 kHz sine wave signal applied.

Group Delay

Group delay is a measure of the absolute time delay between when an input is sampled by the converter to when the result associated with that sample is available to be read back from the ADC, including delay induced by the analog front end of the device. It is measured by applying a step response to the analog inputs and obtaining the impulse response of the entire converter.

Group Delay Drift

Group delay drift is the change in group delay per unit temperature across the entire operating temperature of the device.

Group Delay Matching

For each simultaneously sampled pair, the group delay matching is the amount of variation in group delay between the two channels.

THEORY OF OPERATION

CONVERTER DETAILS

The AD7616 is a data acquisition system that employs a high speed, low power, charge redistribution, successive approximation analog-to-digital converter (ADC) and allows dual simultaneous sampling of 16 analog input channels. The analog inputs on the AD7616 can accept true bipolar input signals. Analog input range options include ± 10 V, ± 5 V and ± 2.5 V. The AD7616 operates from a single 5 V supply.

The AD7616 contains input clamp protection, input signal scaling amplifiers, a first-order antialiasing filter, an on-chip reference, reference buffer, dual high speed ADC, a digital filter, flexible sequencer, and high speed parallel and serial interfaces.

The AD7616 can be operated in hardware or software mode by controlling the HW_RNGSELx pins. In hardware mode, the AD7616 is configured by pin control. In software mode, the AD7616 is configured by the control registers accessed via the serial or parallel interface.

ANALOG INPUT

Analog Input Channel Selection

The AD7616 contains dual simultaneous sampling 16-bit ADCs. Each ADC has 8 analog input channels for a total of 16 analog inputs. Additionally the AD7616 has on-chip diagnostic channels to monitor the V_{CC} supply and on-chip ALDO regulator. Channels can be selected for conversion by control of the CHSELx pins in hardware mode or via the channel register control in software mode. Software mode is required to sample the diagnostic channels. Channels can be selected dynamically or the AD7616 has an on-chip sequencer to allow the channels for conversion to be preprogrammed. In hardware mode, simultaneous sampling is limited to the corresponding A and B channel, that is, Channel VA0 is always sampled with Channel VB0. In software mode, it is possible to select any A channel with any B channel for simultaneous sampling.

Analog Input Ranges

The AD7616 can handle true bipolar, single-ended input voltages. The logic levels on the range select pins, HW_RNGSEL0 and HW_RNGSEL1, determine the analog input range of all analog input channels. If both range select pins are tied to a logic low, the analog input range is determined in software mode via the input range registers (see the Register Summary section for more details). In software mode, it is possible to configure an individual analog input range per channel.

Table 8. Analog Input Range Selection

Analog Input Range	HW_RNGSEL1	HW_RNGSEL0
Configured via the Input Range Registers	0	0
± 2.5 V	0	1
± 5 V	1	0
± 10 V	1	1

In hardware mode, a logic change on these pins has an immediate effect on the analog input range; however, there is typically a settling time of approximately 120 μ s in addition to the normal acquisition time requirement. The recommended practice is to hardwire the range select pins according to the desired input range for the system signals.

During normal operation, the applied analog input voltage must remain within the analog input range selected via the range select pins.

Analog Input Impedance

The analog input impedance of the AD7616 is 1 M Ω . This is a fixed input impedance that does not vary with the AD7616 sampling frequency. This high analog input impedance eliminates the need for a driver amplifier in front of the AD7616, allowing for direct connection to the source or sensor.

Analog Input Clamp Protection

Figure 8 shows the analog input structure of the AD7616. Each analog input of the AD7616 contains clamp protection circuitry. Despite single 5 V supply operation, this analog input clamp protection allows for an input over voltage of up to ± 20 V.

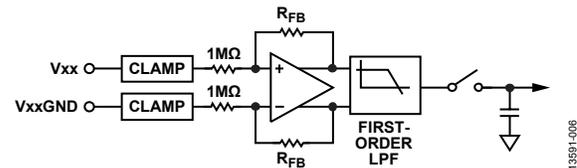


Figure 8. Analog Input Circuitry

Figure 9 shows the current vs. voltage characteristic of the clamp circuit. For input voltages of up to ± 20 V, no current flows in the clamp circuit. For input voltages that are above ± 20 V, the AD7616 clamp circuitry turns on.

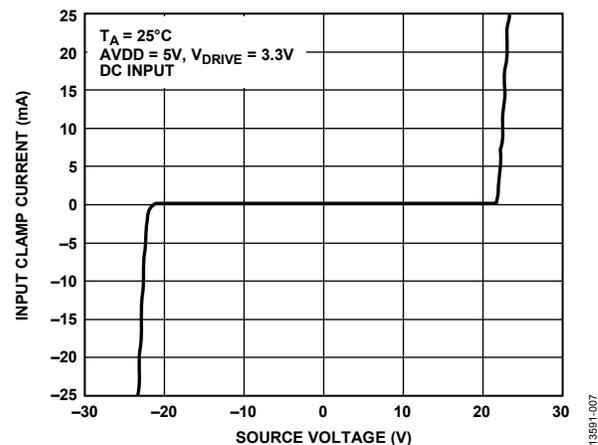


Figure 9. Input Protection Clamp Profile

Place a series resistor on the analog input channels to limit the current to ± 10 mA for input voltages above ± 20 V. In an application where there is a series resistance on an analog input channel, V_{Ax} or V_{Bx} , a corresponding resistance is required on the analog input ground channel, V_{AxGND} or V_{BxGND} (see Figure 10). If there is no corresponding resistor on the V_{AxGND} or V_{BxGND} channel, an offset error occurs on that channel. It is recommended that the input overvoltage clamp protection circuitry be used to protect the AD7616 against transient overvoltage events. It is not recommended to leave the AD7616 in a condition where the clamp protection circuitry is active in normal or power-down conditions for extended periods.

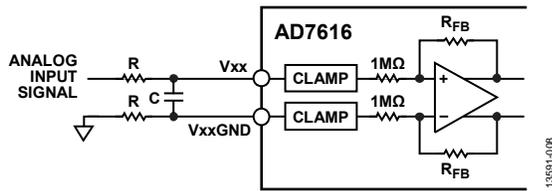
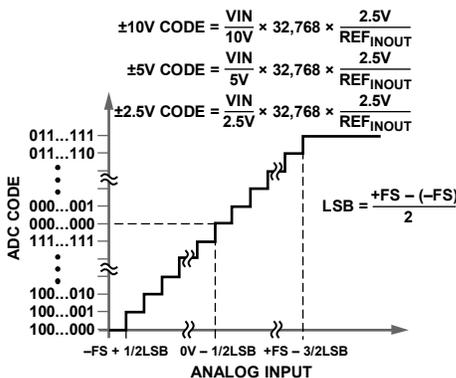


Figure 10. Input Resistance Matching on the Analog Input

ADC TRANSFER FUNCTION

The output coding of the AD7616 is twos complement. The designed code transitions occur midway between successive integer LSB values, that is, $1/2$ LSB and $3/2$ LSB. The LSB size is $FSR/65,536$ for the AD7616. The ideal transfer characteristic for the AD7616 is shown in Figure 11. The LSB size is dependent on the analog input range selected.



	+FS	MIDSCALE	-FS	LSB
±10V RANGE	+10V	0V	-10V	305 μ V
±5V RANGE	+5V	0V	-5V	152 μ V
±2.5V RANGE	+2.5V	0V	-2.5V	76 μ V

Figure 11. Transfer Characteristics

INTERNAL/EXTERNAL REFERENCE

The AD7616 can operate with either an internal or external reference. The device contains an on-chip 2.5 V band gap reference. The REFINOUT pin allows access to the 2.5 V reference that generates the on-chip 4.096 V reference internally, or it allows an external reference of 2.5 V to be applied to the AD7616. An externally applied reference of 2.5 V is also gained up to 4.096 V using the internal buffer. This 4.096 V buffered reference is the reference used by the SAR ADC.

The REFSEL pin is a logic input pin that allows the user to select between the internal reference and an external reference. If this pin is set to logic high, the internal reference is selected and enabled. If this pin is set to logic low, the internal reference is disabled and an external reference voltage must be applied to the REFINOUT pin.

The internal reference buffer is always enabled. After a full reset, the AD7616 operates in the reference mode selected by the REFSEL pin. Decoupling is required on the REFINOUT pin for both the internal and external reference options. A 100 nF ceramic capacitor is required on the REFINOUT pin to REFINOUTGND.

The AD7616 contains a reference buffer configured to gain the reference voltage up to ~ 4.096 V. A ceramic capacitor of 10 μ F is required between REFCAP and REFGND. The reference voltage available at the REFINOUT pin is 2.5 V. When the AD7616 is configured in external reference mode, the REFINOUT pin is a high input impedance pin.

If the internal reference is to be applied elsewhere within the system then it must first be buffered externally.

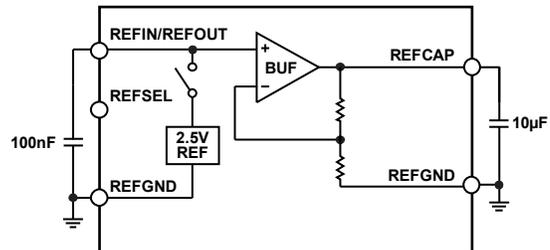


Figure 12. Reference Circuitry

SHUTDOWN MODE

The AD7616 enters shutdown mode by keeping the RESET pin low for greater than 1.2 μ s. When the RESET pin is set from low to high, the device exits shutdown mode and enters normal mode.

When the AD7616 is placed in shutdown mode, the current consumption is typically 150 μ A and the power-up time to perform a write to the device is approximately 0.24 ms. Power-up time to perform a conversion is 15 ms. In shutdown mode, all circuitry is powered down.

DIGITAL FILTER

The AD7616 contains an optional digital first-order sinc filter that must be used in applications where slower throughput rates are used or where higher signal-to-noise ratio or dynamic range is desirable.

The oversampling ratio (OSR) of the digital filter is controlled in hardware using the oversampling pins, OS2 to OS0 (OSx), or in software via the OS bits within the configuration register. In software mode, oversampling is enabled for all channels after the OS bits are set in the configuration register. In hardware mode, the OSx signals at the time full reset is released determine the OSR to be used.

Table 9 provides the oversampling bit decoding to select the different oversample rates. In addition to the oversampling function, the output result is decimated to 16-bit resolution.

If the OSx pins/OS bits are set to select an OS ratio of eight, the next CONVST rising edge takes the first sample for the selected channel, and the remaining seven samples for that channel are taken with an internally generated sampling signal. These samples are then averaged to yield an improvement in SNR performance. As the OS ratio increases, the -3 dB frequency is reduced, and the allowed sampling frequency is also reduced. The conversion time extends as the oversampling rate is increased, and the BUSY signal scales with oversampling rates. Acquisition and conversion time increase linearly with oversampling ratio.

If oversampling is enabled with the sequencer or in burst mode, the extra samples are gathered for a given channel before the sequencer moves on to the next channel.

Table 9 shows the typical SNR performance of the device for each permissible oversampling ratio. The input tone used was a 100 Hz sine wave for the three input ranges of the device. A plot of SNR vs. oversampling ratio (OSR) can be seen in Figure 13.

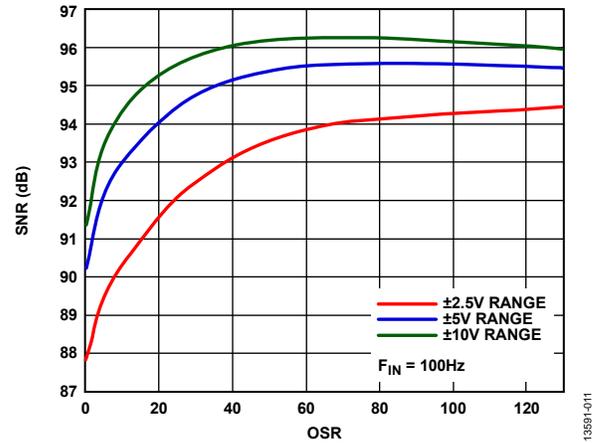


Figure 13. Typical SNR vs. OSR for all Analog Input Ranges

Table 9. Oversampling Bit Decoding

OSx Pins/OS Bits	OS Ratio	SNR (dB)			-3 dB BW (kHz)
		±2.5 V Range	±5 V Range	±10 V Range	All Ranges
000	No OS	87.5	89.7	90.8	35
001	2	88.1	90.6	91.8	32.7
010	4	89	91.6	92.9	31.7
011	8	89.9	92.6	93.9	29.3
100	16	91	93.6	94.9	23
101	32	92.6	94.8	95.8	14.7
110	64	93.9	95.5	96.2	8.3
111	128	94.4	95.4	95.9	4.3

FUNCTIONALITY OVERVIEW

The AD7616 has two main modes of operation, hardware mode and software mode. Additionally the communications interface for hardware or software mode can be via either a serial or a parallel interface. Depending on the mode of operation and interface chosen, certain functionality may not be available. Full

functionality is available in both software serial and software parallel mode with restricted functionality in hardware serial mode and hardware parallel mode. Table 10 outlines the functionality available in the different modes of operation.

Table 10. Functionality Matrix

Functionality	Operation Mode ¹			
	Software Mode, HW_RNGSELx = 00		Hardware Mode, HW_RNGSELx ≠ 00	
	Serial, SER/PAR = 1	Parallel, SER/PAR = 0	Serial, SER/PAR = 1	Parallel, SER/PAR = 0
Internal/External Reference	Yes	Yes	Yes	Yes
Selectable Analog Input Ranges				
Individual Channel Configuration	Yes	Yes	No	No
Common Channel Configuration	No	No	Yes	Yes
Sequential Sequencer	Yes	Yes	Yes	Yes
Fully Configurable Sequencer	Yes	Yes	No	No
Burst Mode	Yes	Yes	Yes	Yes
On-Chip Oversampling	Yes	Yes	Yes	No
CRC	Yes	Yes	Yes	No
Diagnostic Channel Conversion	Yes	Yes	No	No
Hardware Reset	Yes	Yes	Yes	Yes
Serial 1-Wire	Yes	No	Yes	No
Serial 2-Wire	Yes	No	Yes	No
Register Access	Yes	Yes	No	No

¹ Yes means available; no means not available.

DEVICE CONFIGURATION

OPERATIONAL MODE

The mode of operation, hardware mode or software mode, is configured when the AD7616 is released from full reset. The logic level of the HW_RNGSELx pins when the RESET pin transitions from low to high determines the operational mode. The HW_RNGSELx pins are dual function. If HW_RNGSELx = 0b00 then the AD7616 enters software mode. Any other combination of the HW_RNGSELx configures the AD7616 to hardware mode and the analog input range is configured as per Table 8. After software mode is configured, the logic level of the HW_RNGSELx signals is ignored. After an operational mode is configured, a full reset via the RESET pin is required to exit the operational mode and set up an alternative mode. If hardware mode is selected, all further device configuration is via pin control. Access to the on-chip registers is prohibited in hardware mode. In software mode, the interface and reference configuration must be configured via pin control but all further device configuration is via register access only.

INTERNAL/EXTERNAL REFERENCE

The internal reference is enabled or disabled when the AD7616 is released from a full reset. The logic level of the REFSEL signal when the RESET pin transitions from low to high configures the reference. After the reference is configured, changes to the logic level of the REFSEL signal are ignored. If the REFSEL signal is set to 1, the internal reference is enabled. If REFSEL is set to Logic 0, the internal reference is disabled and an external reference must be supplied to the REFINOUT pin for correct operation of the AD7616. A full reset via the RESET pin is required to exit the operational mode and set up an alternative mode.

Connect a 100 nF capacitor between the REFINOUT and REFINOUTGND pins. If using an external reference, place a 10 kΩ band limiting resistor in series between the reference and the REFINOUT pin of the AD7616.

DIGITAL INTERFACE

The digital interface selection, parallel or serial, is configured when the AD7616 is released from full reset. The logic level of the SER/PAR signal when the RESET pin transitions from low to high configures the interface. If the SER/PAR signal is set to 0, the parallel interface is enabled. If the SER/PAR signal is set to 1, the serial interface is selected. Additionally, if the serial interface is selected, the SER1W signal is monitored when the RESET pin is released to determine if serial 1-wire or 2-wire mode is selected. After the interface is configured, changes to the logic level of the SER/PAR signal, or in the case where serial interface is enabled the SER1W signal, are ignored. A full reset via the RESET pin is required to exit the operation mode and set up an alternative mode.

HARDWARE MODE

If hardware mode is selected, the available functionality is restricted and all functionality is configured via pin control. The logic level of the following signals is checked after a full reset to configure the functionality of the AD7616: CRC, BURSTEN, SEQEN, and OSx. Table 11 provides a summary of the signals that are latched by the device on the release of a full reset, depending on the mode of operation chosen. After the device configuration is configured, a full reset via the RESET pin is required to exit the configuration and set up an alternative configuration. Functionality availability is restricted depending on the interface type selected. Consult Table 10 for a full list of the functionality available in hardware parallel or serial mode.

The CHSELx pins are queried at reset to determine the initial analog input channel pair to acquire for conversion or to configure the initial settings for the sequencer. The channel pair selected for conversion or the hardware sequencer can be reconfigured during normal operation by setting and maintaining the CHSELx signal level before the CONVST rising edge until the BUSY falling edge.

The HW_RNGSELx signals control the analog input range for all 16 analog input channels. A logic change on these pins has an immediate effect on the analog input range; however, the typical settling time is approximately 120 μs, in addition to the normal acquisition time requirement. The recommended practice is to hardwire the range select pins according to the desired input range for the system signals.

Access to the on-chip registers is prohibited in hardware mode.

SOFTWARE MODE

If software mode is selected and the reference and interface type is configured, all other configuration settings in the AD7616 are controlled via the on-chip registers. All functionality of the AD7616 is available when software mode is selected. Table 11 provides a summary of the signals that are latched by the device on the release of a full reset, depending on the mode of operation chosen.

Table 11. Summary of Latched Hardware Signals

Signal	Latched at Full Reset		Read at Reset		Read During Busy		Interrupt Driven	
	HW Mode	SW Mode	HW Mode	SW Mode	HW Mode	SW Mode	HW Mode	SW Mode
REFSEL	Yes	Yes						
SEQEN	Yes	No						
HW_RNGSELx (Range Change)			Yes	Yes			Yes	No
HW_RNGSELx (Hardware (HW) or Software (SW) Mode)	Yes	Yes						
SER/ $\overline{\text{PAR}}$	Yes	Yes						
CRCEN	Yes	No						
OSx	Yes	No						
Burst	Yes	No						
CHSELx			Yes	No	Yes	No		
$\overline{\text{SER1W}}$	Yes	Yes						

RESET FUNCTIONALITY

The AD7616 has two reset modes: full or partial. The reset mode selected is dependent on the length of the reset low pulse. A partial reset requires 50 ns to complete and a full reset requires 15 ms to completely reconfigure the device after release of the RESET signal.

A partial reset reinitializes the following modules:

- Sequencer
- Digital filter
- SPI interface
- Both SAR ADCs

The current conversion result is discarded on completion of a partial reset. The partial reset does not affect the register values programmed in software mode, or the latches that store the user configuration in both hardware and software modes. A dummy conversion is required in software mode after a partial reset.

A full reset returns the device to its default power-on state. The following are configured when the AD7616 is released from full reset:

- Hardware mode or software mode
- Internal/external reference
- Interface type

On power-up, the $\overline{\text{RESET}}$ signal can be released as soon as both the VCC and V_{DRIVE} supplies are stable. The logic level of the

HW_RNGSELx, REFSEL, SER/ $\overline{\text{PAR}}$ and $\overline{\text{SER1W}}$ pins when the RESET pin is released after a full reset determine the configuration.

If hardware mode is selected, the functionality determined by the CRC, BURSTEN, SEQEN and OSx signals is also latched when the RESET pin transitions from low to high in full reset mode. After the functionality is configured, changes to these signals are ignored. In hardware mode, the analog input range (HW_RNGSELx signals) can be configured during either a full or partial reset or during normal operation, but hardware/software mode selection requires a full reset to reconfigure as this setting is latched.

In hardware mode, the CHSELx and HW_RNGSELx pins are queried at release from both full and partial RESET to

- Determine the initial analog input channel pair to acquire for conversion.
- Configure the initial settings for the sequencer.
- Select the analog input voltage range.

These signals are not latched. The channel pair selected for conversion, or the hardware sequencer, can be reconfigured during normal operation by setting and maintaining the CHSELx signal level before the CONVST rising edge, and ensuring it the signal level remains constant until after BUSY transitions low again. See the Channel Selection section for further details.

In software mode, all additional functionality is configured via controlling the on-chip registers.

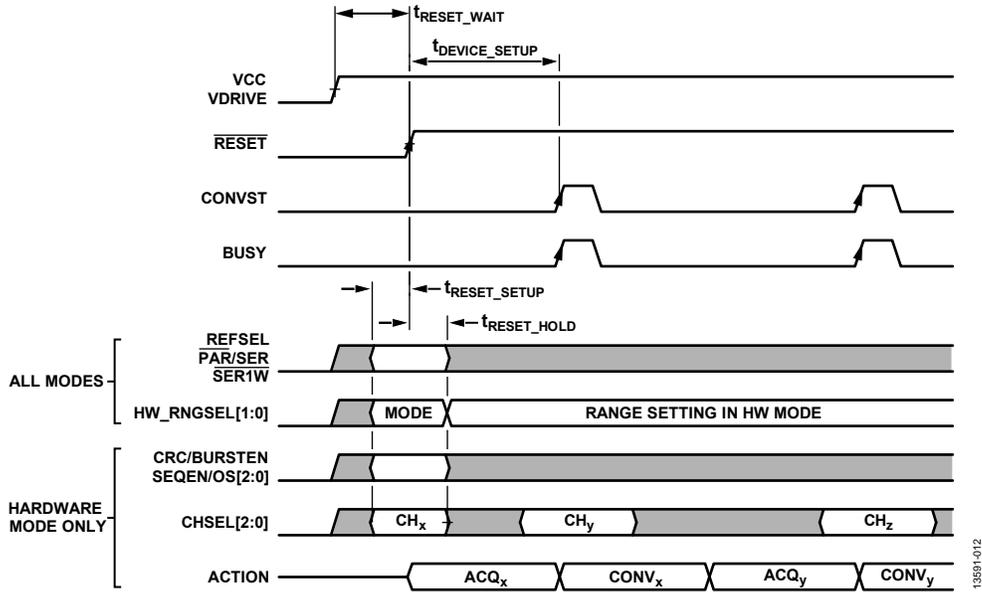


Figure 14. AD7616 Configuration at Reset

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PIN FUNCTION OVERVIEW

There are several dual function pins on the AD7616. Their functionality is dependent on the mode of operation selected by

the HW_RNGSELx pins. Table 12 outlines the pin functionality in the different modes of operation and interface modes.

Table 12. Pin Functionality Overview

Pins	Operation Mode			
	Software, HW_RNGSELx = 00		Hardware, HW_RNGSELx ≠ 00	
	Serial, SER/PAR = 1	Parallel, SER/PAR = 0	Serial, SER/PAR = 1	Parallel, SER/PAR = 0
CHSELx	No function, connect to GND		CHSELx	
SCLK/RD	SCLK	R \overline{D}	SCLK	R \overline{D}
WR/BURST	Connect to GND	WR	BURST	Connect to GND
DB15 to DB13, OSx	Connect to GND	DB[15:13]	OSx	Connect to GND
DB12/SDOA	SDOA	DB[12]	SDOA	SDOA
DB11/SDOB	SDOB, leave floating for serial 1-wire mode	DB[11]	SDOB	SDOB, leave floating for serial 1-wire mode
DB10/SDI	SDI	DB[10]	Connect to GND	SDI
DB9 to DB6, DB3 to DB0	Connect to GND	DB[9:6], DB[3:0]	Connect to GND	Connect to GND
DB5/CRCEN	Connect to GND	DB5	CRCEN	Connect to GND
DB4/SER1W	SER1W	DB4	SER1W	SER1W
HW_RNGSELx	HW_RNGSELx, connect to GND		HW_RNGSELx, configure analog input range	
SEQEN	No function, connect to GND		SEQEN	
REFSEL	REFSEL			

DIGITAL INTERFACE

CHANNEL SELECTION

Hardware Mode

The logic level of the CHSELx signals determine the channel pair for conversion; see Table 13 for signal decoding information. The CHSELx signals at the time that either full or partial reset is released determine the initial channel pair to sample. After a reset, the logic levels of the CHSELx signals are examined during the BUSY high period to set the channel pair for the next conversion. The CHSELx signal level may be set before CONVST goes from low to high and be maintained until BUSY goes from high to low to indicate a conversion is complete. See Figure 15 for further details.

Software Mode

In software mode, the channels for conversion are selected by control of the channel register. On power-up or after a reset, the default channels selected for conversion are channel VA0 and VB0.

Table 13. CHSELx Pin Decoding

Channel Selection Input Pin			Analog Input Channels for Conversion
CHSEL0	CHSEL1	CHSEL2	
0	0	0	VA0, VB0
0	0	1	VA1, VB1
0	1	0	VA2, VB2
0	1	1	VA3, VB3
1	0	0	VA4, VB4
1	0	1	VA5, VB5
1	1	0	VA6, VB6
1	1	1	VA7, VB7

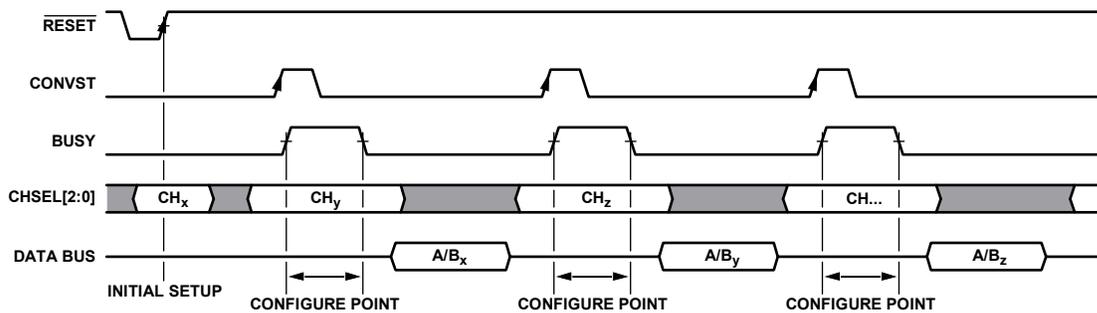


Figure 15. Hardware Mode Channel Conversion Setting

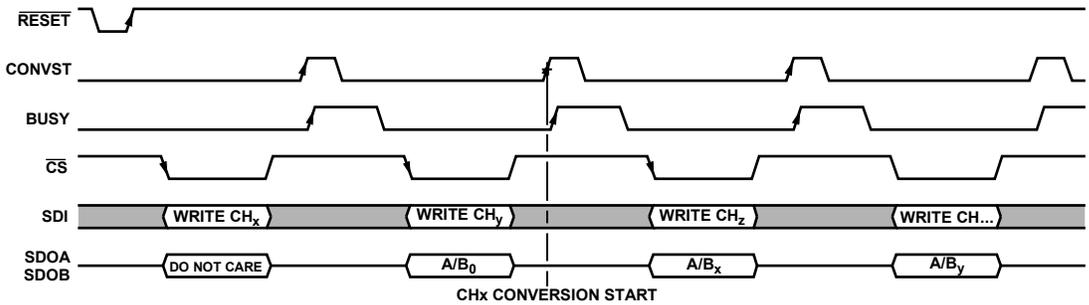


Figure 16. Software Serial Mode Channel Conversion Setting

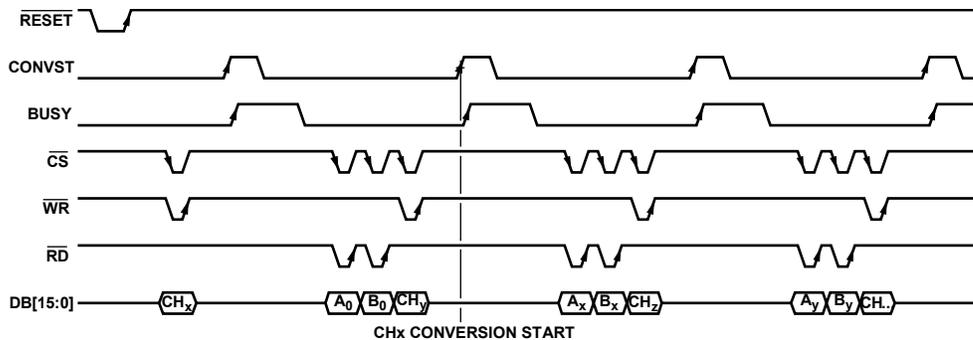


Figure 17. Software Parallel Mode Channel Conversion Setting

PARALLEL INTERFACE

The parallel interface reads conversion results and to configure and read back the on-chip registers. Data can be read from the AD7616 via the parallel data bus with standard $\overline{\text{CS}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$ signals. To read the data over the parallel bus, tie the $\overline{\text{SER/PAR}}$ pin low.

Reading Conversion Results

The CONVST signal initiates the conversion process. A low to high transition on the CONVST signal initiates a conversion of the selected inputs. The BUSY signal goes high to indicate a conversion is in progress. When the BUSY signal transitions from high to low to indicate that a conversion is complete it is possible to read back conversion results on the parallel interface.

Data can be read from the AD7616 via the parallel data bus with standard $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals. The $\overline{\text{CS}}$ and $\overline{\text{RD}}$ input signals are internally gated to enable the conversion result onto the data bus. The data lines, DB15 to DB0, leave their high impedance state when both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are logic low.

The rising edge of the $\overline{\text{CS}}$ input signal three-states the bus, and the falling edge of the $\overline{\text{CS}}$ input signal takes the bus out of the high impedance state. $\overline{\text{CS}}$ is the control signal that enables the data lines; it is the function that allows multiple AD7616 devices to share the same parallel data bus.

The number of required read operations depends on the device configuration. A minimum of two reads are required to read the conversion result for the simultaneously sampled A and B channels. If additional functions such as CRC, status or Burst mode is enabled the number of required read backs increases accordingly.

The $\overline{\text{RD}}$ pin reads data from the output conversion results register. Applying a sequence of $\overline{\text{RD}}$ pulses to the $\overline{\text{RD}}$ pin of the AD7616 clocks the conversion results out from each channel onto the parallel bus DB15 to DB0. The first $\overline{\text{RD}}$ falling edge after BUSY goes low clocks out the conversion result from Channel A_x. The next $\overline{\text{RD}}$ falling edge updates the bus with the Channel B_x conversion result.

Writing Register Data

In software mode, all the read/write registers in the AD7616 can be written to over the parallel interface. A register write command is performed by a single 16-bit parallel access via the parallel bus DB15 to DB0, $\overline{\text{CS}}$ and $\overline{\text{WR}}$ signals. Data written to the AD7616 should be provided on the DB15 to DB0 inputs, with DB0 being the LSB of the data-word. The format for a write command is shown in Figure 21. Bit D15 must be set to 1 to select a write command. Bits[D14:D9] contain the register address. The subsequent nine bits (Bits[D8:D0]) contain the data to be written to the selected register. See the Register Summary section for the complete list of register addresses. Data is latched into the device on the rising edge of $\overline{\text{WR}}$.

Reading Register Data

All the registers in the device can be read over the parallel interface. A register read is performed by first writing the address of the register to read to the AD7616. The format for a register read command is shown in Figure 23. Bit D15 must be set to 0 to select a read command. Bits[D14:D9] contain the register address. The subsequent nine bits (Bits[D8:D0]) are ignored. The read command is latched into the AD7616 on the rising edge of $\overline{\text{WR}}$. This transfers the relevant register data to the output register. The register data can then be read on the DB[15:0] pins by using a standard read command. See Figure 23 for additional information.

SERIAL INTERFACE

To interface to the AD7616 over the serial interface, the $\overline{\text{PAR/SER}}$ pin must be tied high. The $\overline{\text{CS}}$ and SCLK signals transfer data from the AD7616. The AD7616 has two serial data output pins, SDOA and SDOB. Data is read back from the AD7616 using serial 1-wire or serial 2-wire mode.

In serial 2-wire mode for the AD7616, conversion results from Channel VA0 to Channel VA7 appear on SDOA, and conversion results from Channel VB0 to Channel VB7 appear on SDOB. In serial 1-wire mode, conversion results from Channels VB0 to VB7 are interlaced with conversion results from Channels VA0 to VA7. To achieve the maximum throughput, it is required to use 2-wire mode.

To read back data over both SDOA and SDOB, the $\overline{\text{SER1W}}$ pin must be tied high. If data is to be read back over SDOA only, the $\overline{\text{SER1W}}$ pin must be tied low. Serial 1-wire or 2-wire mode is configured when the AD7616 is released from full reset.

Reading Conversion Results

The CONVST signal initiates the conversion process. A low to high transition on the CONVST signal initiates a conversion of the selected inputs. The BUSY signal goes high to indicate a conversion is in progress. When the BUSY signal transitions from high to low to indicate that a conversion is complete, it is possible to read back conversion results on the serial interface.

The $\overline{\text{CS}}$ falling edge takes the data output lines, SDOA and SDOB, out of three-state and clocks out the MSB of the conversion result. The rising edge of SCLK clocks all subsequent data bits onto the serial data outputs, SDOA and SDOB. Figure 19 shows a read of two simultaneous conversion results using two SDO lines on the AD7616. If the status register is appended to the conversion results or operating in sequencer burst mode where multiples of 16 SCLK transfers access data from the AD7616, $\overline{\text{CS}}$ may be held low to frame the entire data. Data can also be clocked out using just one SDO line, in which case SDOA must be used to access all conversion data. For the AD7616 to access both channel VAx and VBx conversion results on one SDO line, a total of 32 SCLK cycles are required. These 32 SCLK cycles can be framed by one $\overline{\text{CS}}$ signal, or each group of 16 SCLK cycles can be individually framed by the $\overline{\text{CS}}$ signal. The disadvantage of using just one SDO line is that the throughput rate is reduced.

Leave the unused SDOB line unconnected in serial 1-wire mode. If SDOA is to be used as a single serial data output line, the channel results are output in the following order: V_{Ax} and V_{Bx}. Figure 20 shows a 1-wire serial read back.

The speed at which the data can be read back in serial interface mode is dependent on SPI frequency, V_{DRIVE} supply, and the capacitance of the load on the SDO line, C_{LOAD}. Table 14 shows a summary of the maximum speed achievable for various conditions.

Table 14. SPI Frequency vs. Load Capacitance

V _{DRIVE} (V)	C _{LOAD} (pF)	SPI Frequency (MHz)
2.3 to 2.7	20	40
2.7 to 3	10	50
2.7 to 3	20	40
3 to 3.6	15	50
3.6 to 5.25	20	50

Writing Register Data

All the read/write registers in the AD7616 can be written to over the serial interface. A register write command is performed by a single 16-bit SPI access. The format for a write command is shown in Table 15. Bit D15 must be set to 1 to select a write command. Bits[D14:D9] contain the register address. The subsequent nine bits (Bits[D8:D0]) contain the data to be written to the selected register. Figure 22 shows a typical serial write command.

Reading Register Data

All the registers in the device can be read over the serial interface. A register read is performed by issuing a register read command followed by an additional SPI command that can be either a valid command or NOP. The format for a read command is shown in Table 16. Bit D15 must be set to 0 to select a read command. Bits[D14:D9] contain the register address. The subsequent nine bits (Bits[D8:D0]) are ignored. See the register section for the complete list of register addresses.

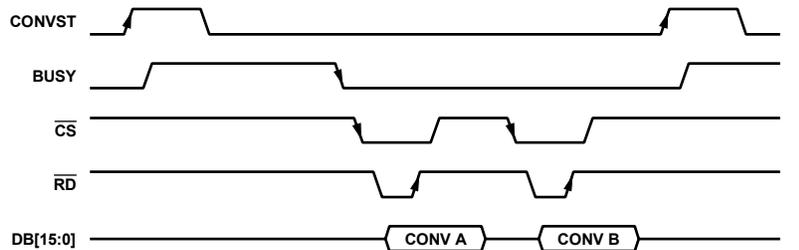


Figure 18. Parallel Interface Conversion Readback

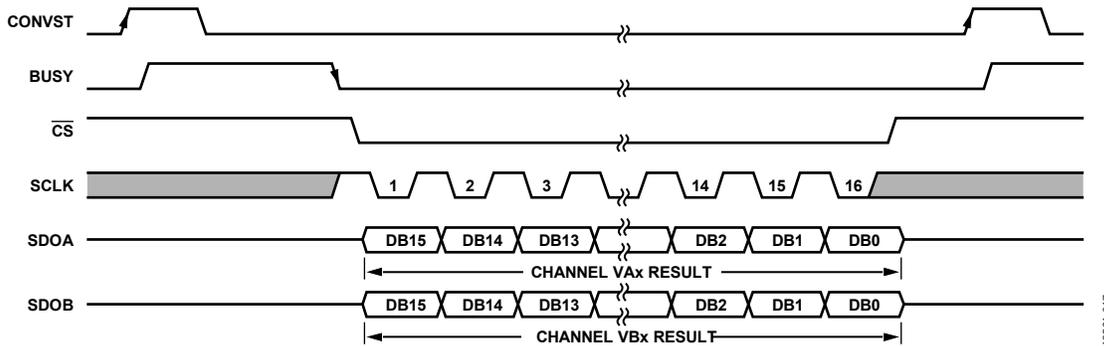


Figure 19. Serial Interface 2-Wire

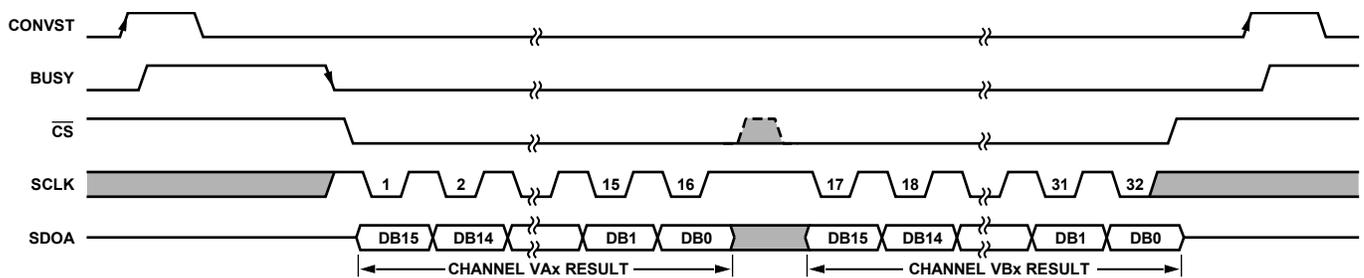


Figure 20. Serial Interface 1-Wire

Table 15. Write Command Message Configuration

MSB														LSB	
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
WR	REG ADDR[5:0]						DATA[8:0]								
1	Register address						Data to write								

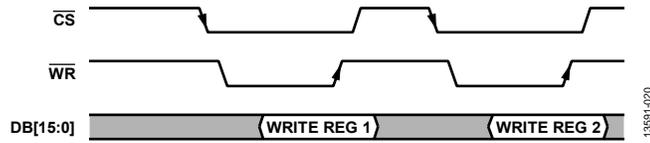


Figure 21. Parallel Interface Register Write

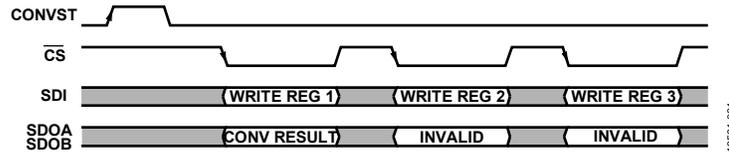


Figure 22. Serial Interface Register Write

Table 16. Read Command Message Configuration

MSB														LSB	
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
WR	REG ADDR[5:0]						DATA[8:0]								
0	Register address						Do not care								

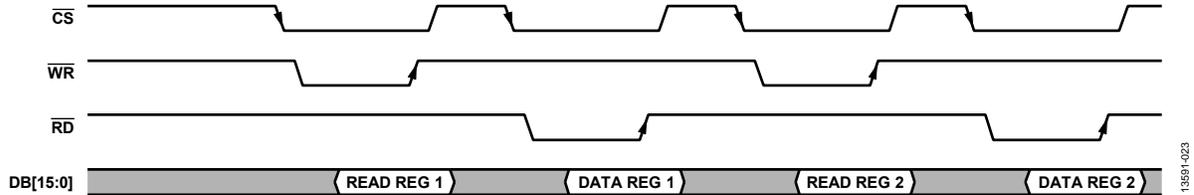


Figure 23. Parallel Interface Register Read

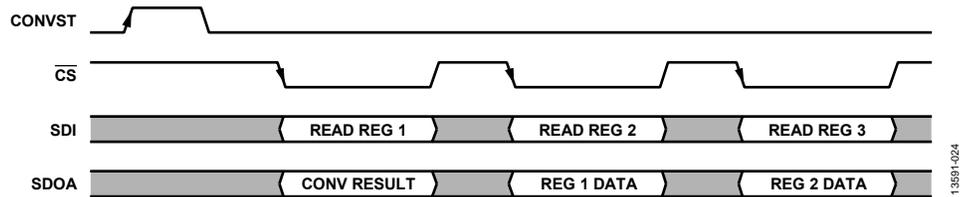


Figure 24. Serial Interface Register Read

SEQUENCER

The AD7616 has a highly configurable on-chip sequencer. The functionality and configuration of the sequencer is dependent on the mode of operation of the AD7616.

In hardware mode, the sequencer is sequential only. The sequencer always starts converting at Channel VA0 and Channel VB0 and converts each subsequent channel up to the configured end channel.

In software mode, the sequencer has additional functionality and configurability. The sequencer stack has 32 uniquely configurable sequence steps allowing any channel order to be programmed. Additionally, any Channel VAx input can be paired with any Channel VBx input or diagnostic channel.

The sequencer can be operated with or without the burst function enabled. With the burst function enabled, only one CONVST pulse is required to convert every channel in a sequence. With burst mode disabled, one CONVST pulse is required for every conversion step in the sequence. See the Burst Sequencer section for additional details on operating in burst mode.

HARDWARE MODE SEQUENCER

In hardware mode, the sequencer is controlled by the SEQEN pin and the CHSELx pins. The sequencer is enabled or disabled when the AD7616 is released from full reset. The logic level of the SEQEN pin when the RESET pin is released determines if the sequencer is enabled or disabled (see Table 17 for settings). After the RESET pin is released, the function is fixed and a full reset via the RESET pin is required to exit the function and set up an alternative configuration.

Table 17. Hardware Mode Sequencer Configuration

SEQEN	Interface Mode
0	Sequencer disabled
1	Sequencer enabled

When the sequencer is enabled the logic levels of the CHSELx pins determine the channels selected for conversion in the sequence. The CHSELx pins at the time RESET is released determines the initial settings for the channels to convert in the sequence. To reconfigure the channels selected for conversion after RESET, set the CHSELx pins to the required setting at the last BUSY pulse before the current conversion sequence is completed. See Figure 25 for further details.

Table 18. CHSELx Pin Decoding Sequencer

Channel Selection Input Pin			Analog Input Channels for Sequential Conversion
CHSEL0	CHSEL1	CHSEL2	
0	0	0	Vx0 only
0	0	1	Vx0 to Vx1
0	1	0	Vx0 to Vx2
0	1	1	Vx0 to Vx3
1	0	0	Vx0 to Vx4
1	0	1	Vx0 to Vx5
1	1	0	Vx0 to Vx6
1	1	1	Vx0 to Vx7

SOFTWARE MODE SEQUENCER

In software mode, the AD7616 contains a 32 deep fully configurable sequencer stack. Control of the sequencer is achieved by programming the configuration register and sequencer stack registers via the parallel or serial interface.

Each stack step can be individually programmed to pair any input from Channel VAx to any input from Channel VBx or any diagnostic channel can be selected for conversion. The sequencer depth can be set to any length from 1 to 32. The sequencer depth is controlled via the SSREN bit. Set the SSREN bit in the sequencer register corresponding to the last step required. The channels to convert are selected by programming the ASELx and BSELx bits in each sequence stack register for the depth required.

The sequencer is activated by setting the SEQEN bit in the configuration register to 1.

To configure and enable the sequencer, it is recommended to complete the following procedure (see Figure 26):

1. Configure the analog input range for the required analog input channels.
2. Program the sequencer stack registers to select the channels for the sequence.
3. Set the EN bit in the last required sequence step.
4. Set the SEQEN bit in the configuration register.
5. Provide a dummy CONVST pulse.
6. Cycle through CONVST pulses and conversion reads to step through the each element of the sequencer stack.

The sequence automatically restarts from the first element in the sequencer stack with the next CONVST pulse.

Following a partial reset, the sequencer pointer is repositioned to the first layer of the stack, but the register programmed values remain unchanged.

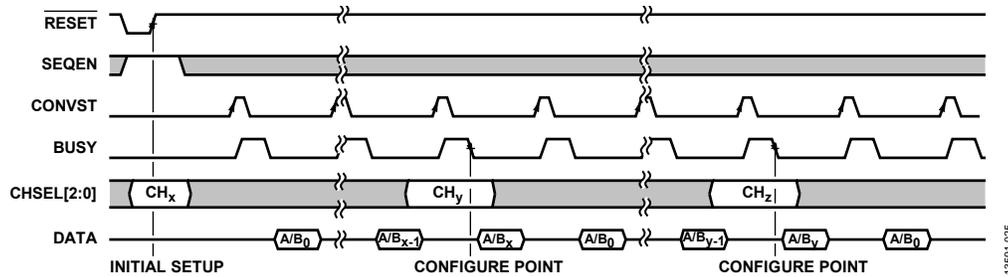


Figure 25. Hardware Mode Sequencer Configuration

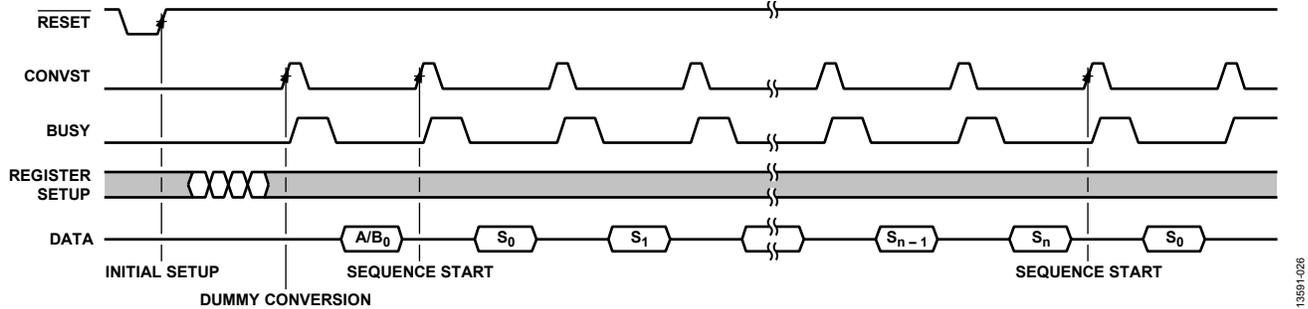


Figure 26. Software Mode Sequencer Configuration

BURST SEQUENCER

Burst mode saves generating a CONVST pulse for each step in a sequence of conversions. One CONVST pulse converts every step in the sequence.

The burst sequencer is an additional feature that works in conjunction with the sequencer. If the burst function is enabled, one CONVST pulse initiates a conversion of all the channels configured in the sequencer. The burst function saves generating a CONVST pulse for each step in a sequence of conversions as is the case if the burst function is disabled.

Configuration of burst function varies depending on the mode of operation: hardware or software mode. See the Hardware Mode Burst section or Software Mode Burst section for specific details on configuring the burst function in the each mode.

When configured, the burst sequence is initiated at the rising edge of CONVST. The BUSY pin goes high to indicate that a conversion is in progress. The BUSY pin remain high until all conversions in the sequence are complete. The conversion results are available for read back after the BUSY pin goes low.

The number of data reads required to read all the data in the burst sequence is dependent on the length of the sequence configured. The conversion results are presented on the data bus, parallel or serial, in the order of conversions that are set up.

Hardware Mode Burst

Burst mode is enabled in hardware mode by setting the BURST pin to 1. The SEQEN pin must also be set to 1 to enable the sequencer.

In hardware mode, the burst sequencer is controlled by the BURST, SEQEN, and CHSELx pins. The burst sequencer is enabled or disabled when the AD7616 is released from full reset. The logic level of the SEQEN pin and the BURST pin when the RESET pin is released determines if the burst sequencer is enabled or disabled. After the RESET pin is released, the function is fixed and a full reset via the RESET pin is required to exit the function and set up an alternative configuration.

When the burst sequencer is enabled, the logic levels of the CHSELx pins determine the channels selected for conversion in the burst sequence. The CHSELx pins at the time RESET is released determines the initial settings for the channels to convert in the burst sequence. To reconfigure the channels selected for conversion after RESET, set the CHSELx pins to the required setting at the next BUSY pulse (see Figure 27 for further details).

Software Mode Burst

In software mode, the burst function is enabled by setting the BURST bit in the configuration register to 1. This action must be performed when setting the SEQEN bit in the configuration register as outlined in the steps to configure the sequencer. See Figure 28 and the Software Mode Sequencer section for additional information.

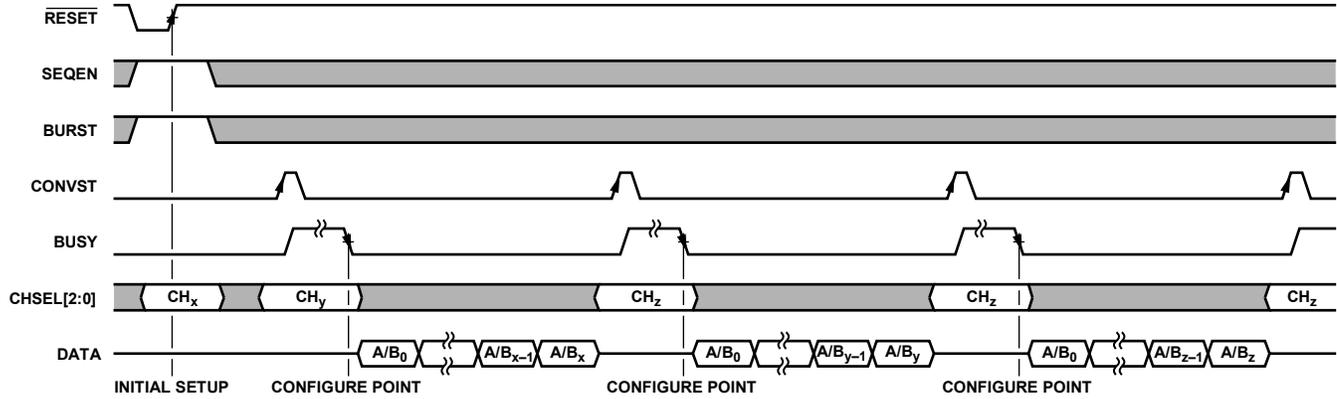


Figure 27. BURST Sequencer Hardware Mode

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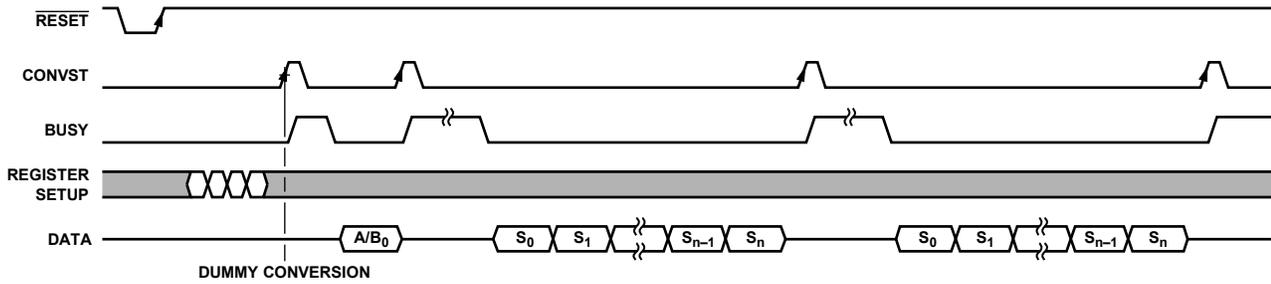


Figure 28. BURST Sequencer Software Mode

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DIAGNOSTICS

DIAGNOSTIC CHANNELS

In addition to the 16 analog inputs, V_{Ax} and V_{Bx}, the AD7616 can also convert the following diagnostic channels: V_{CC} and the analog ALDO voltage. The diagnostic channels are selected for conversion by programming the channel register (see the Channel Register section) to the corresponding channel identifier. Diagnostic channels may also be added to the sequencer stack in software mode, but only provide an accurate reading at throughput rates <250 kSPS. See Figure 31 for a plot of the typical accuracy vs. throughput rate that can be expected when using the diagnostic channels.

The expected output for each channel is governed by the following transfer functions,

$$V_{CC} \text{ Code} = \frac{((4 \times V_{CC}) - V_{REF}) \times 32,768}{5 \times V_{REF}} + 32,768$$

$$LDO \text{ Code} = \frac{((10 \times V_{ALDO}) - (7 \times V_{REF})) \times 32,768}{10 \times V_{REF}} + 32,768$$

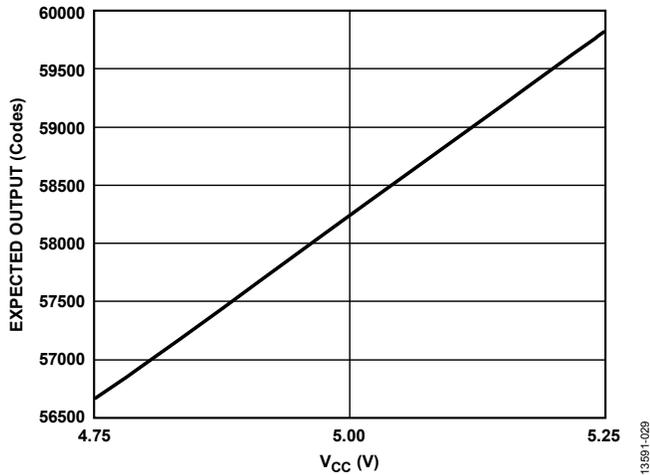


Figure 29. VCC Diagnostic Transfer Function

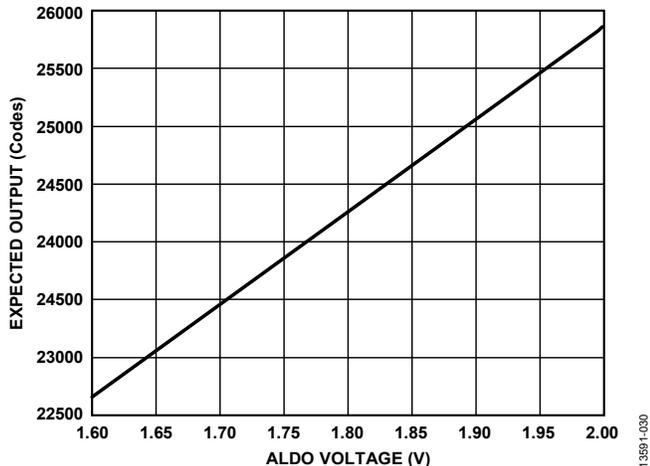


Figure 30. ALDO Diagnostic Transfer Function

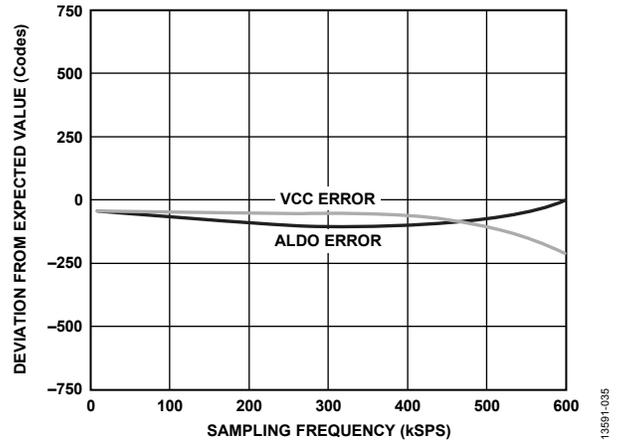


Figure 31. Diagnostic Accuracy vs. Throughput

INTERFACE SELF TEST

It is possible to test the integrity of the digital interface by selecting the communication self test channel in the channel register (see the Channel Register section).

Selecting the communication self test for conversion forces the conversion result register to a known fixed output. When conversion code is read, Code 0xA555 is output as the conversion code of Channel A, and Code 0x5555 is output as the conversion code of Channel B.

CRC

The AD7616 has a cyclic redundancy check (CRC) checksum mode that can be used to improve interface robustness by detecting errors in data. The CRC feature is available in both software (serial and parallel) mode and hardware (serial only) mode. The CRC feature is not available in hardware parallel mode. The CRC result is contained within the status register. Enabling the CRC feature enables the status register and vice versa.

In hardware mode, the CRCEN pin controls the CRC feature. The CRC feature is enabled or disabled when the AD7616 is released from full reset. The logic level of the CRCEN pin when the RESET pin is released determines if the CRC feature is enabled or disabled. Set the CRCEN pin to 1 to enable the CRC feature. After the RESET pin is released the function is fixed and a full reset via the RESET pin is required to exit the function and set up an alternative configuration. See the Reset Functionality section for additional information. After enabled, the CRC result is appended to the conversion result and consists of a 16-bit word where the first 8 bits contain the channel ID (CHID) of the last channel pair converted and the last 8 bits are the CRC result. The result is accessed via an extra read command, as shown in Figure 32.

In software mode, the CRC function is enabled by setting either the CRCEN bit, or the STATUSEN bit, in the configuration register to 1 (see the Configuration Register section).

If the CRC function is enabled, a CRC is calculated on the conversion results for Channel V_{Ax} and Channel V_{Bx}. The CRC is calculated and transferred on the serial or parallel interface after the conversion results are transmitted, depending on the configuration of the device.

The following is a description of how the CRC is implemented in the AD7616:

```
crc = 8'b0;
i = 0;
x = number of conversion channel pairs;
for (i=0, i<x, i++) begin
  crc1 = crc_out(An,Crc);
  crc = crc_out(Bn,Crc1);
  i = i +1;
end
```

where the function `crc_out(data, crc)` is

```
crc_out[0] = data[14] ^ data[12] ^ data[8] ^
data[7] ^ data[6] ^ data[0] ^ crc[0] ^
crc[4] ^ crc[6];
```

```
crc_out[1] = data[15] ^ data[14] ^ data[13]
^ data[12] ^ data[9] ^ data[6] ^ data[1] ^
data[0] ^ crc[1] ^ crc[4] ^ crc[5] ^ crc[6]
^ crc[7];
```

```
crc_out[2] = data[15] ^ data[13] ^ data[12]
^ data[10] ^ data[8] ^ data[6] ^ data[2] ^
data[1] ^ data[0] ^ crc[0] ^ crc[2] ^ crc[4]
^ crc[5] ^ crc[7];
```

```
crc_out[3] = data[14] ^ data[13] ^ data[11]
^ data[9] ^ data[7] ^ data[3] ^ data[2] ^
data[1] ^ crc[1] ^ crc[3] ^ crc[5] ^ crc[6];
```

```
crc_out[4] = data[15] ^ data[14] ^ data[12]
^ data[10] ^ data[8] ^ data[4] ^ data[3] ^
data[2] ^ crc[0] ^ crc[2] ^ crc[4] ^ crc[6]
^ crc[7];
```

```
crc_out[5] = data[15] ^ data[13] ^ data[11]
^ data[9] ^ data[5] ^ data[4] ^ data[3] ^
crc[1] ^ crc[3] ^ crc[5] ^ crc[7];
```

```
crc_out[6] = data[14] ^ data[12] ^ data[10]
^ data[6] ^ data[5] ^ data[4] ^ crc[2] ^
crc[4] ^ crc[6];
```

```
crc_out[7] = data[15] ^ data[13] ^ data[11]
^ data[7] ^ data[6] ^ data[5] ^ crc[3] ^
crc[5] ^ crc[7];
```

The initial CRC word used by the AD7616 is an 8-bit word equal to zero. The XOR operation described above is carried out to calculate each bit of the CRC word for the conversion result, A_N. This CRC word (crc1) is then used as the starting point for calculating the CRC word (crc) for the conversion result, B_N. The process repeats cyclically for each channel pair converted.

Depending on the mode of operation of the AD7616, the status register value is appended to the conversion data and read out via an extra read command over the serial or parallel interface. The user can then repeat the calculation described above, for the received conversion results, to check if both CRC words match. See Figure 32 for a description of how the CRC word is appended to the data for each mode of operation.

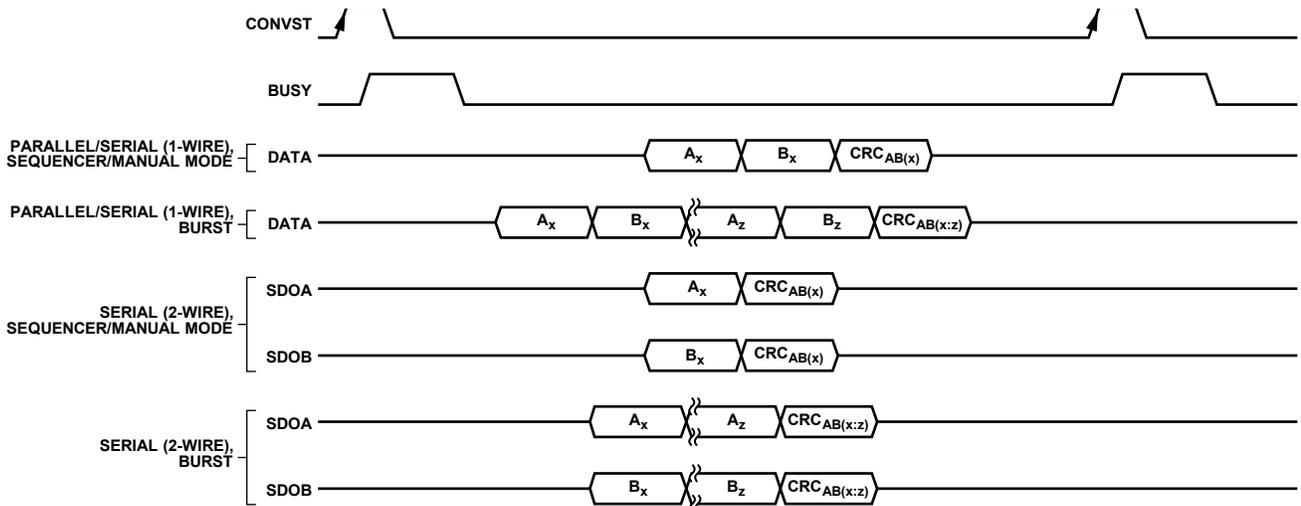


Figure 32. CRC Readback for All Modes

13891-032

REGISTER SUMMARY

The AD7616 has six read/write registers used for configuring the device in software mode, 32 sequencer stack registers for programming the flexible on-chip sequencer and a read-only status register. Table 19 shows an overview of the read/write registers available on the AD7616. The status register is an additional read only register than contains information on the previous channel pair converted and the CRC result.

Table 19. Register Summary

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x02	Configuration register	[15:8]	Addressing							Reserved	0x0000	R/W
		[7:0]	SDEF	BURSTEN	SEQEN	OS		STATUSEN	CRCEN			
0x03	Channel register	[15:8]	Addressing							Reserved	0x0000	R/W
		[7:0]	CHB				CHA					
0x04	Input Range Register A1	[15:8]	Addressing							Reserved	0x00FF	R/W
		[7:0]	VA3		VA2		VA1		VA0			
0x05	Input Range Register A2	[15:8]	Addressing							Reserved	0x00FF	R/W
		[7:0]	VA7		VA6		VA5		VA4			
0x06	Input Range Register B1	[15:8]	Addressing							Reserved	0x00FF	R/W
		[7:0]	VB3		VB2		VB1		VB0			
0x07	Input Range Register B2	[15:8]	Addressing							Reserved	0x00FF	R/W
		[7:0]	VB7		VB6		VB5		VB4			
0x20 to 0x3F	Sequencer Stack Registers [0:31]	[15:8]	Addressing							SSRENx	0x0000 ¹	R/W
		[7:0]	BSELx				ASELx					
N/A	Status register	[15:8]	A[3:0]				B[3:0]				N/A	R
		[7:0]	CRC[7:0]									

¹ After a full or partial rest is issued, the sequencer stack register is reinitialized to cycle through Channel VA0 and Channel VB0 to Channel VA7 and Channel VB7. The remaining 24 layers of the stack are reinitialized to 0x0.

ADDRESSING REGISTERS

The seven MSBs written to the device are decoded to determine which register is addressed. The seven MSBs consist of the register address (REGADDR) Bits[5:0] and the read/write bit. The register address bits determine which on-chip register is selected. The read/write bit determines if the remaining nine

bits of data on the SDI/DBx lines are loaded into the addressed register. If the read/write bit is 1, the bits load into the register addressed by the register select bits. If the read/write bit is 0, the command is seen as a read request. The addressed register data is available to be read during the next read operation.

MSB							LSB								
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W/R	REG ADDR[5]	REG ADDR[4]	REG ADDR[3]	REG ADDR[2]	REG ADDR[1]	REG ADDR[0]	DATA[8:0]								

Table 20.

Bit	Mnemonic	Description
D15	W/R	If a 1 is written to this bit then Bits[D8:D0] of this register are written to the register specified by REGADDR[5:0]. Alternatively, if a 0 is written the next operation is a read from the designated register.
D14	REGADDR[5]	If a 1 is written to this bit, the contents of REGADDR[4:0] specifies the 32 Sequencer Stack Registers. Alternatively is a 0 is written to this bit, a register is selected as defined by REGADDR[4:0].
D13 to D9	REGADDR[4:0]	When W/R = 1, the contents of REGADDR[4:0] determine register for selection as follows: 00001: reserved. 00010: selects the configuration register. 00011: selects the channel register. 00100: selects the Input Range Register A1. 00101: selects the Input Range Register A2. 00110: selects the Input Range Register B1. 00111: selects the Input Range Register B2.. 01000: selects the status register When W/R = 0, and REGADDR[4:0] contains 00000, the conversion codes are read.
D8 to D0	DATA[8:0]	These bits are written into the corresponding register specified by bits REGADDR[5:0]. See the following sections for detailed descriptions of each register.

CONFIGURATION REGISTER

The configuration register is used in software mode to configure many of the main functions of the ADC, including the sequencer, burst mode, oversampling, and CRC options.

Address: 0x02, Reset: 0x0000, Name: Configuration Register

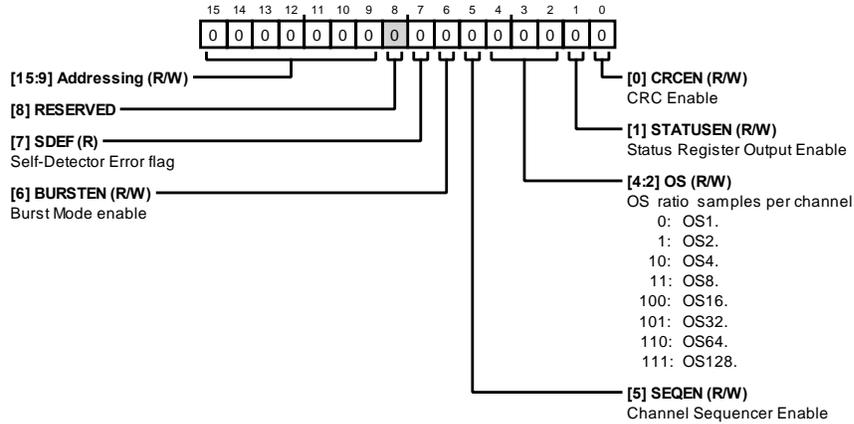


Table 21. Bit Descriptions for Configuration Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing	0	Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	RW
8	RESERVED		Reserved.	0x0	R/W
7	SDEF	0 1	Self-detect error flag. 0 Test passed. The AD7616 has configured itself successfully after power-up. 1 Test failed. An issue was detected during device configuration. A reset is required.	N/A	R
6	BURSTEN	0 1	Burst mode enable. 0 Burst mode is disabled. Each channel pair to be converted requires a CNVST pulse. 1 A single CNVST pulse converts every channel pair programmed in the 32-layer sequencer stack registers up to and including the layer defined by the SSREN bit. See the Software Mode Sequencer section and the Software Mode Burst section for further details.	0x0	RW
5	SEQEN	0 1	Channel sequencer enable. 0 The channel sequencer is disabled. 1 The channel sequencer is enabled.	0x0	RW
[4:2]	OS2, OS1, OS0	000 001 010 011 100 101 110 111	Oversampling ratio. 000 Oversampling disabled. 001 Oversampling enabled, OSR = 2. 010 Oversampling enabled, OSR = 4. 011 Oversampling enabled, OSR = 8. 100 Oversampling enabled, OSR = 16. 101 Oversampling enabled, OSR = 32. 110 Oversampling enabled, OSR = 64. 111 Oversampling enabled, OSR = 128.	0x0	RW
1	STATUSEN	0 1	Status register output enable. 0 The status register is not read out when reading the conversion result. 1 The status register is read out at the end of all the conversion words (including the self test channel if enabled in sequencer mode) of all the selected channels are read out. The CRC result is included in the last 8 bits.	0x0	RW
0	CRCEN		The STATUSEN and CRCEN bits have identical functionality.	0x0	RW

CHANNEL REGISTER

Address: 0x03, Reset: 0x0000, Name: Channel Register

In software manual mode, the Channel Register selects the input channel or self-test channel for the next conversion.

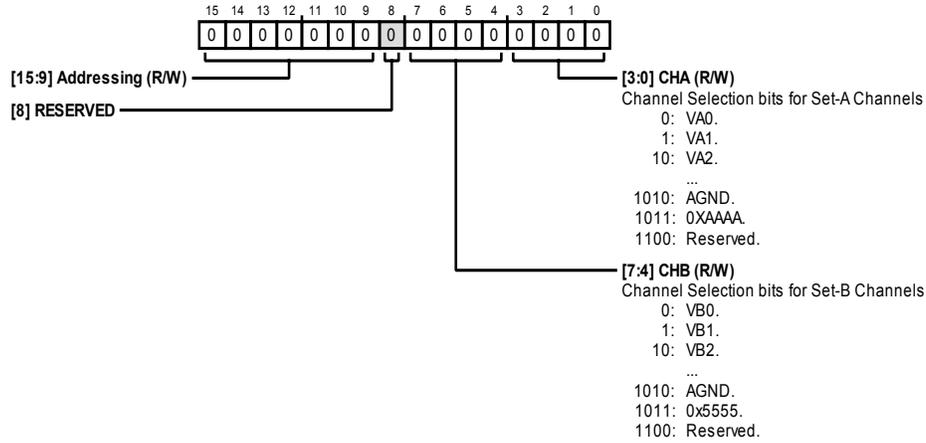


Table 22. Bit Descriptions for Channel Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
8	RESERVED		Reserved.	0x0	R/W
[3:0]	CHA		Channel selection bits for Set B Channels.	0x0	R/W
[7:4]	CHB	0000	VA0/VB0.		
		0001	VA1/VB1.		
		0010	VA2/VB2.		
		0011	VA3/VB3.		
		0100	VA4/VB4.		
		0101	VA5/VB5.		
		0110	VA6/VB6.		
		0111	VA7/VB7.		
		1000	V _{CC} .		
		1001	ALDO.		
		1010	Reserved.		
		1011	Set the dedicated bits for digital interface communication self test function. When conversion codes are read, Code 0xA000 is read out as the conversion code of Channel A, and Code 0x5555 is output as the conversion code of Channel B.		
		1100	Reserved.		

INPUT RANGE REGISTERS

Input Range Register A1 and Input Range Register A2 select from one of the three possible input ranges ($\pm 10\text{ V}$, $\pm 5\text{ V}$ or $\pm 2.5\text{ V}$) for analog input Channel VA0 to Channel VA7. Input Range Register B1 and Input Range Register B2 select from one of the three possible input ranges ($\pm 10\text{ V}$, $\pm 5\text{ V}$ or $\pm 2.5\text{ V}$) for analog input Channel VB0 to Channel VB7.

INPUT RANGE REGISTER A1

Address: 0x04, Reset: 0x00FF, Name: Input Range Register A1

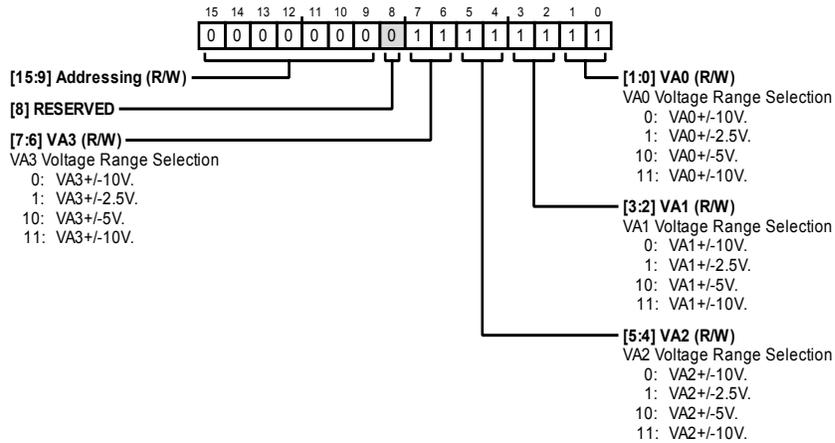


Table 23. Bit Descriptions for Input Range Register A1

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
8	RESERVED		Reserved	0x0	R/W
[7:6]	VA3	0 1 10 11	VA3 voltage range selection. VA3 $\pm 10\text{ V}$. VA3 $\pm 2.5\text{ V}$. VA3 $\pm 5\text{ V}$. VA3 $\pm 10\text{ V}$.	0x3	R/W
[5:4]	VA2	0 1 10 11	VA2 voltage range selection. VA2 $\pm 10\text{ V}$. VA2 $\pm 2.5\text{ V}$. VA2 $\pm 5\text{ V}$. VA2 $\pm 10\text{ V}$.	0x3	R/W
[3:2]	VA1	0 1 10 11	VA1 voltage range selection. VA1 $\pm 10\text{ V}$. VA1 $\pm 2.5\text{ V}$. VA1 $\pm 5\text{ V}$. VA1 $\pm 10\text{ V}$.	0x3	R/W
[1:0]	VA0	0 1 10 11	VA0 voltage range selection. VA0 $\pm 10\text{ V}$. VA0 $\pm 2.5\text{ V}$. VA0 $\pm 5\text{ V}$. VA0 $\pm 10\text{ V}$.	0x3	R/W

INPUT RANGE REGISTER A2

Address: 0x05, Reset: 0x00FF, Name: Input Range Register A2

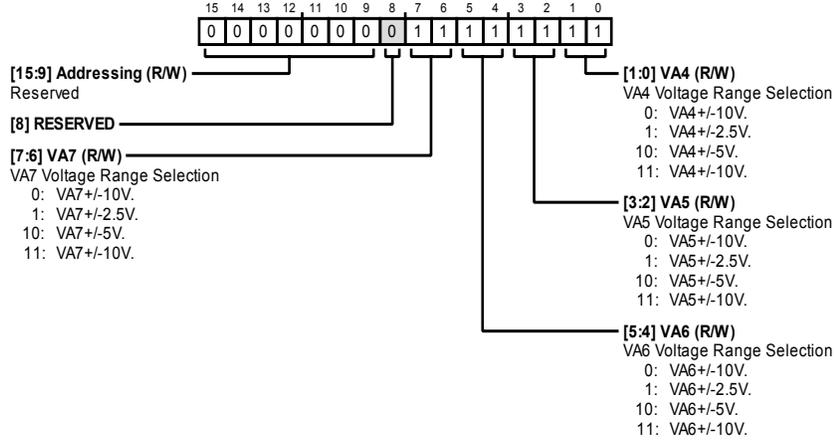


Table 24. Bit Descriptions for Input Range Register A2

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
8	RESERVED		Reserved	0x0	R/W
[7:6]	VA7	0 1 10 11	VA7 voltage range selection. VA7 ± 10 V. VA7 ± 2.5 V. VA7 ± 5 V. VA7 ± 10 V.	0x3	R/W
[5:4]	VA6	0 1 10 11	VA6 voltage range selection. VA6 ± 10 V. VA6 ± 2.5 V. VA6 ± 5 V. VA6 ± 10 V.	0x3	R/W
[3:2]	VA5	0 1 10 11	VA5 voltage range selection. VA5 ± 10 V. VA5 ± 2.5 V. VA5 ± 5 V. VA5 ± 10 V.	0x3	R/W
[1:0]	VA4	0 1 10 11	VA4 voltage range selection. VA4 ± 10 V. VA4 ± 2.5 V. VA4 ± 5 V. VA4 ± 10 V.	0x3	R/W

INPUT RANGE REGISTER B1

Address: 0x06, Reset: 0x00FF, Name: Input Range Register B1

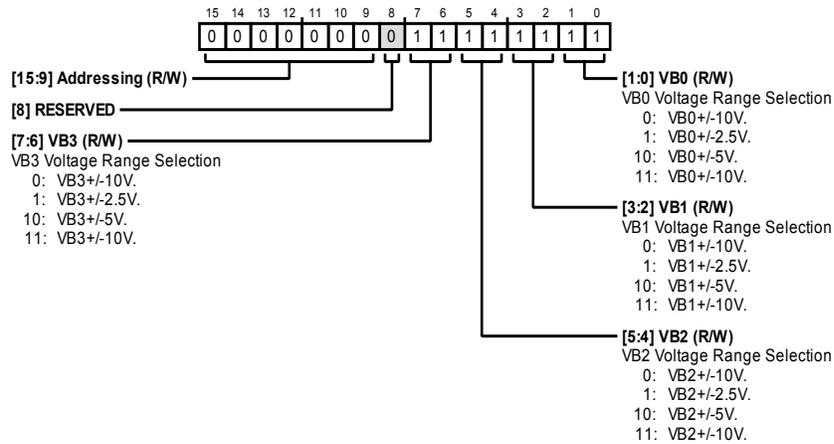
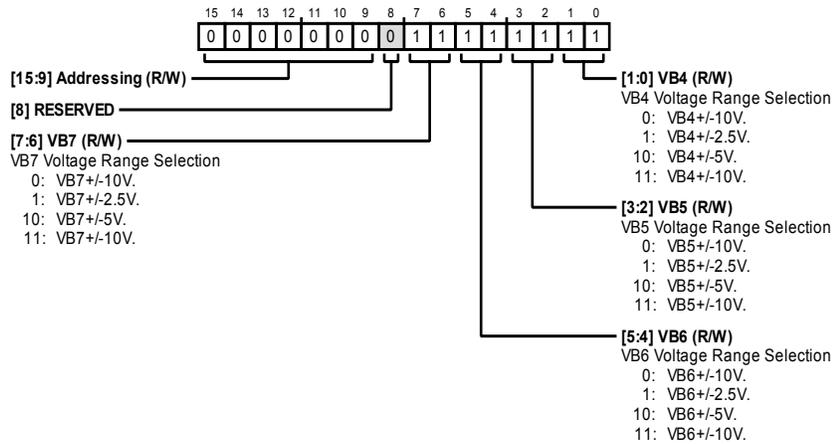


Table 25. Bit Descriptions for Input Range Register B1

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
8	RESERVED		Reserved	0x0	R/W
[7:6]	VB3	0 1 10 11	VB3 voltage range selection. VB3 ± 10 V. VB3 ± 2.5 V. VB3 ± 5 V. VB3 ± 10 V.	0x3	R/W
[5:4]	VB2	0 1 10 11	VB2 voltage range selection. VB2 ± 10 V. VB2 ± 2.5 V. VB2 ± 5 V. VB2 ± 10 V.	0x3	R/W
[3:2]	VB1	0 1 10 11	VB1 voltage range selection. VB1 ± 10 V. VB1 ± 2.5 V. VB1 ± 5 V. VB1 ± 10 V.	0x3	R/W
[1:0]	VB0	0 1 10 11	VB0 voltage range selection. VB0 ± 10 V. VB0 ± 2.5 V. VB0 ± 5 V. VB0 ± 10 V.	0x3	R/W

INPUT RANGE REGISTER B2

Address: 0x07, Reset: 0x00FF, Name: Input Range Register B2

**Table 26. Bit Descriptions for Input Range Register B2**

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
8	RESERVED		Reserved.	0x0	R/W
[7:6]	VB7	0 1 10 11	VB7 voltage range selection. VB7 ± 10V. VB7 ± 2.5V. VB7 ± 5V. VB7 ± 10V.	0x3	R/W
[5:4]	VB6	0 1 10 11	VB6 voltage range selection. VB6 ± 10V. VB6 ± 2.5V. VB6 ± 5V. VB6 ± 10V.	0x3	R/W
[3:2]	VB5	0 1 10 11	VB5 voltage range selection. VB5 ± 10V. VB5 ± 2.5V. VB5 ± 5V. VB5 ± 10V.	0x3	R/W
[1:0]	VB4	0 1 10 11	VB4 voltage range selection. VB4 ± 10V. VB4 ± 2.5V. VB4 ± 5V. VB4 ± 10V.	0x3	R/W

SEQUENCER STACK REGISTERS

Although the channel register can define the next channel for conversion (be it a diagnostic channel or pair of analog input channels), if the user wants to sample numerous analog input channels, the 32 sequencer stack registers offer a convenient solution. Within the communication register, when the REGADDR5 bit is set to Logic 1, the contents of REGADDR[4:0] specifies 1 of the 32 sequencer stack registers. Within each sequencer stack register, the user can define a pair of analog inputs to sample simultaneously.

The structure of the sequence forms a stack, in which each row represents two channels to convert simultaneously. The sequence begins with Sequencer Stack Register 1 and cycles through to Sequencer Stack Register 32. If Bit D8 (the enable bit SSRENx) within a sequencer stack register is set to 1, the sequence ends with the pair of analog inputs defined by that register and then returns to the first sequencer stack register and resumes the cycle again. By default, the sequencer stack registers are programmed to cycle through Channel VA0 and Channel VB0 through to Channel VA7 and Channel VB7. After a full or partial reset is issued, the sequencer stack register is reinitialized to cycle through Channel VA0 and Channel VB0 to Channel VA7 and Channel VB7.

Address: 0x20 to 0x3F, Reset: 0x0000, Name: Sequencer Stack Registers [0:31]

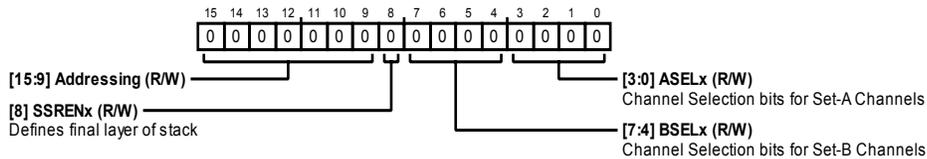


Table 27. Bit Descriptions for Sequencer Stack Register [0:31]

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
8	SSREN[0:31]		Setting this bit to 0 instructs the ADC to move to the next layer of the sequencer stack after converting the present channel pair. Setting this bit to 1 defines that layer of the sequencer stack as the final layer in the sequence. Thereafter, the sequencer loops back to the first layer of the stack.	0x0	R/W
[7:4]	BSEL[0:31]		Channel selection bits for Set B channels.	0x0 ¹	R/W
		0000	VB0.		
		0001	VB1.		
		0010	VB2.		
		0011	VB3.		
		0100	VB4.		
		0101	VB5.		
		0110	VB6.		
		0111	VB7.		
		1000	V _{CC} .		
		1001	ALDO.		
		1010	Reserved.		
		1011	Set the dedicated bits for digital interface communication self test function. When the conversion codes is read, Code 0xAAAA is read out as the conversion code of Channel A, and Code 0x5555 is output as the conversion code of Channel B.		
		1100	Reserved.		
[3:0]	ASEL[0:31]		Channel selection bits for Set A channels. As per above, for V _{Ax} channels.	0x0 ¹	R/W

¹ After a full or partial reset is issued, the sequencer stack register is reinitialized to cycle through Channel VA0 and Channel VB0 to Channel VA7 and Channel VB7. The remaining 24 layers of the stack are reinitialized to 0x0.

STATUS REGISTER

The status register is a 16-bit read only register. If the STATUSEN bit or the CRCEN bit are set to Logic 1 in the configuration register, the status register is read out at the end of all conversion words for the selected channels, including the self test channel if enabled in sequencer mode.

MSB														LSB	
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A[3:0]				B[3:0]				CRC[7:0]							

Table 28. Bit Descriptions for Status Register

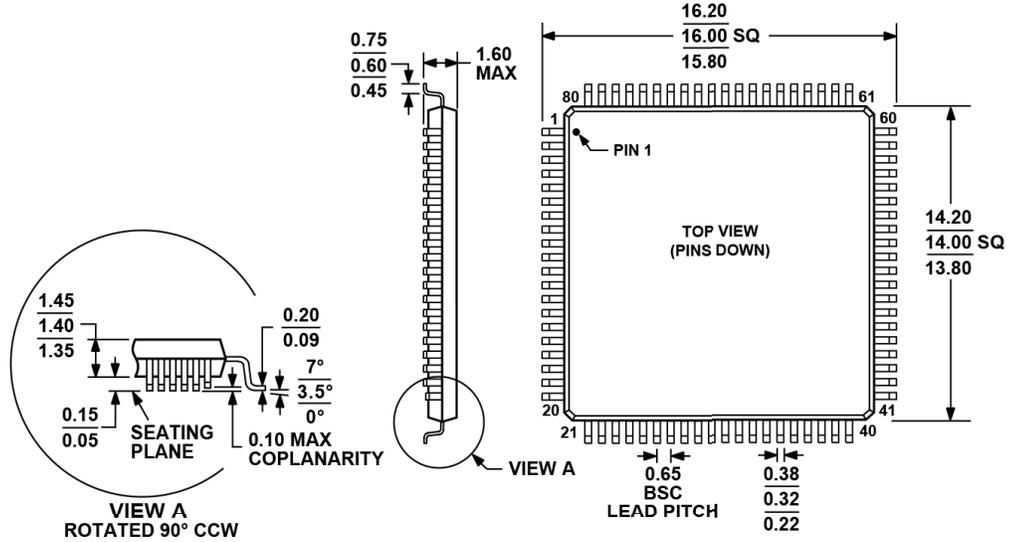
Bit	Bit Name	Settings	Description	Reset	Access
RD15 to D12	A[3:0]		Channel index for previous conversion result on Channel A.	N/A	R
D11 to D8	B[3:0]		Channel index for previous conversion result on Channel B.	N/A	R
D7 to D0	CRC		CRC calculation for the previous conversion result(s). Refer to the CRC section for further details.	N/A	R

OUTLINE DIMENSIONS



80-Lead Low Profile Quad Flat Package [LQFP]
(ST-80-2)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026-BEC

Figure 33. 80-Lead LQFP Package Outline Dimensions